A   Reg. No. : [ ][ ][ ][ ][ ][ ][ ][ ][ ][ ]

Question Paper Code: 53306

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2019

Third Semester

Electrical and Electronics Engineering

15UEE306 -DIGITAL LOGIC CIRCUITS

(Regulation 2015)

Duration: Three hours   Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. Convert binary 111111110010 to hexadecimal.   CO1- R

   (a) $EE2_{16}$ (b) $FF2_{16}$ (c) $2FE_{16}$ (d) $FD2_{16}$

2. Any signed negative binary number is recognized by its _____   CO1- R

   (a) MSB   (b) LSB   (c) Byte   (d) Nibble

3. Canonical form is a unique way of representing _____   CO2- R

   (a) SOP   (b) Minterm   (c) Boolean Expressions   (d) POS

4. The format used to present the logic output for the various combinations of logic inputs to a gate is called   CO2- R

   (a) Truth table.   (b) Input logic function.

   (c) Boolean constant   (d) Boolean variable

5. What is a shift register that will accept a parallel input, or a bidirectional serial load and internal shift features, called?   CO3- R

   (a) Tri state   (b) End around   (c) Universal   (d) Conversion

6. A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates?   CO3- R

   (a) AND or OR   (b) XOR or XNOR   (c) NOR or NAND   (d) AND or NOR

7. Table that is not a part of asynchronous analysis procedure is   CO4- R

   (a) Transition table   (b) State table   (c) Flow table   (d) Excitation table

8. How much locations an 8-bit address code can select in memory?   CO4- R

   (a) 8 locations   (b) 256 locations   (c) 65,536 locations   (d) 131,072 locations

9. Each unit to be modeled in a VHDL design is known as   CO5- R

   (a) Behavioral model   (b) Design architecture

   (c) Design entity   (d) Structural model

10. Which of the following describes the connections between the entity port and   CO5-R
    the local component?
    (a) Port map   (b) One to many map

    (c) One to one map   (d) Many to many map

PART – B (5 x 2= 10 Marks)

11. Why Excess-3 code is called self complementing code?   CO1- U
12. Draw the circuit diagram of full adder using two half adders.   CO2- R
13. Compare Moore and Melay circuits.   CO3- R
14. Define static hazard.   CO4- R
15. What are the various modeling techniques in VHDL?   CO5- R

PART – C (5 x 16= 80 Marks)

16. (a) (i) Encode the binary word 1011 into seven bit even parity CO1- U   (10)
         Hamming Code.

         (ii) Write short notes on binary weighted code.   CO1- U   (6)

                                   Or

    (b) (i) With a neat schematic explain the working of two input CO1- U   (10)
         TTL NAND gate.

         (ii) Compare totem pole and open collector outputs.   CO1- U   (6)

17. (a) Design a 3:8 decoder and explain its operation as a minterm CO2- Ana   (16)
         and maxterm generator.
                                   Or

    (b) Design a circuit that can convert a four bit binary code into its CO2- Ana (16)
         equivalent gray code.

2

53306

18. (a) Design a MOD-7 synchronous counter using JK flip flop and CO3- Ana   (16)
implement it. Also draw its timing diagram.

Or

(b) Design a clocked sequential circuit for the state diagram CO3- Ana   (16)
shown in Fig.1 using T flip flop.
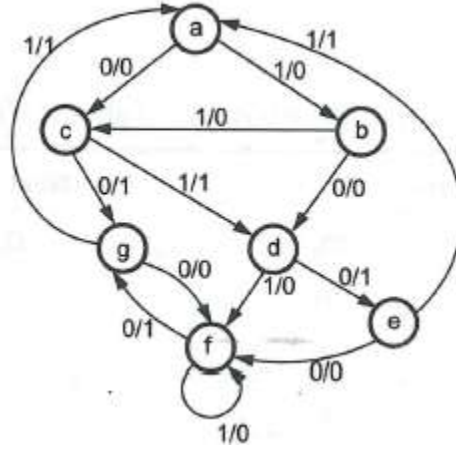

Fig.1

19. (a) (i) Analyze the following asynchronous network shown in   CO4-Ana   (16)
Fig.2 using a flow table. Starting in the total stable state for
which $X = Z = 0$.
(ii) Are there any races in the flow table?

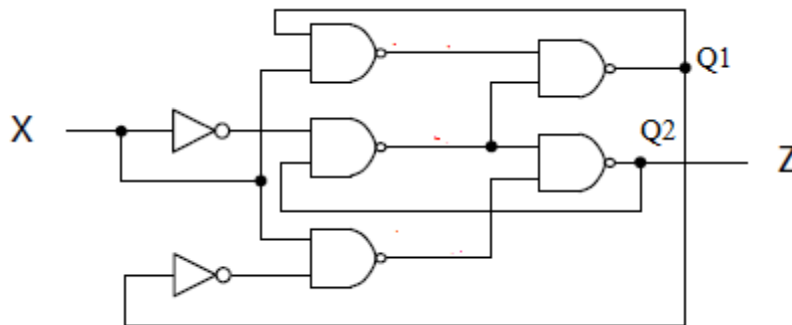
Fig.2

Or

(b) Show how to programme the fusible links to get a 4 bit gray CO4-Ana   (16)
code from the binary inputs using PLA and PAL and compare
the design requirements with PROM.

53306

20. (a) Write a VHDL program for full adder using structural CO5-U (16) modeling and 1: 4 DMUX using data flow modeling.

Or

(b) (i) Explain the various operators supported by VHDL. CO5-U (8)

(ii) Write a VHDL code to realize a decade counter with CO5-U (8) behavioral modeling.

53306