Reg. No. : | | | | | | | | | | |

Question Paper Code: 33402

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2019

Third Semester

Electronics and Communication Engineering

01UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Use Boolean algebra to simplify the function $f = x(y + wz) + wxz$. Sketch the logic circuit for the minimized function using NAND gates.
2. Realize EX-OR Gate from NAND Gate.
3. Write the truth table for full subtractor.
4. Define decoder.
5. Differentiate the combinational logic from sequential logic.
6. What is meant by Shift Register? List its types.
7. State the advantages and disadvantages of TTL.
8. List the different types of memory.
9. What is the difference between synchronous and asynchronous sequential circuits?
10. Distinguish between static and dynamic hazards.

PART - B (5 x 16 = 80 Marks)

11. (a) Simplify the following expression $F(w, x, y, z) = \sum_m (1, 3, 4, 5, 9, 10, 11) + \sum_d (6, 8)$ using Quine – McCluskey method. (16)

Or

(b) Simplify the following function using tabulation method.
$f(A, B, C, D) = \sum m(2, 3, 7, 9, 11, 13) + \sum d(1, 10, 15)$ (16)

12. (a) (i) Implement the full subtractor using a 1: 8 demultiplexer. (6)

(ii) Implement the following Boolean function using 16:1 multiplexer
$f(A, B, C, D, E) = \sum m(2, 4, 5, 7, 10, 14, 15, 16, 17, 25, 26, 30, 31)$ (10)

Or

(b) Design a 4-bit magnitude comparator. (16)

13. (a) Discuss in detail about JK flip flop with its truth table, state diagram and characteristics equation. (16)

Or

(b) Design and draw a 3 bit synchronous counter which goes through the following states: *1 – 3 – 5 – 7 – 1* (16)

14. (a) Implement the following two Boolean functions
$F1(A,B,C) = \sum(0,1,2,4)$
$F2(A,B,C) = \sum(0,5,6,7)$ using
i) PLA ii) PAL iii) ROM (16)

Or

(b) Design a Two-Bit Magnitude Comparator with a PLA. (16)

15. (a) Design an asynchronous sequential circuit with two inputs X and Y and with one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change for any change in X. Use SR latch for implementation of the circuit. (16)

Or

(b) (i) Illustrate with an example the hierarchical modeling concepts used in Verilog HDL. (10)

(ii) Write a Verilog code to perform 4 bit Full Adder with carry look ahead. (6)