C **Reg. No. :** | | | | | | | | | | |

Question Paper Code: 56403

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2019

Sixth Semester

Electronics and Communication Engineering

15UEC603- VLSI DESIGN

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5 Marks)

1. In continuous assignment left hand side must be CO1-R

   (a) Net (b) Reg (c) Scalar or vector net (d) Scalar or vector reg

2. CMOS technology is used in developing CO2-U

   (a) Microprocessors (b) Microcontrollers

   (c) Digital logic circuits (d) all of the mentioned

3. In CMOS circuits, which type of power dissipation occurs due to switching of transient current and charging & discharging of load capacitance? CO3-U

   (a) Static dissipation (b)Dynamic dissipation

   (c) Both a and b (d) None of the above

4. Charge leakage and noise margin problems can be addressed by adding _____ CO4-U

   (a) Keeper circuit (b) domino gate (c) pass transistor (d) transmission gate

5. The number of test vectors for exhaustive testing is calculated by CO5-A

   (a) $2^{(m+n)}$ (b) $2^{((m+n)/2)}$ (c) $2^{(m-n)}$ (d) $2^{2(m+n)}$

PART – B (5 x 3= 15Marks)

6. What are gate primitives? CO1-U

7. Define the lambda layout rules. CO2-R

8. Define logical effort and parasitic delay. CO3-R

9. What is meant by synchronizers. CO4-R

10. What is meant by a test program? CO5-U

PART – C (5 x 16= 80Marks)

11.	(a)	(i) Write a Verilog program for 2 to 4 decoder in dataflow modeling and behavioral modeling.	CO1-U	(8)
		(ii) Write the Verilog code for full adder in structural level modeling with diagram.	CO1-U	(8)
		Or		
	(b)	(i) Explain in detail blocking and non-blocking assignment.	CO1-U	(8)
		(ii) Explain how to represent the gate delays in Verilog HDL.	CO1-U	(8)
12.	(a)	Explain in detail DC transfer characteristic of CMOS inverter	CO2-U	(16)
		Or		
	(b)	Explain the different steps involved in SOI CMOS fabrication process with neat diagrams	CO2-U	(16)
13.	(a)	Analyze the static and dynamic power dissipation in CMOS circuits with necessary diagrams and expressions.	CO3-Ana	(16)
		Or		
	(b)	(i) Discuss the different reliability problems related to the design of reliable CMOS chip	CO3-Ana	(10)
		(ii) Discuss the principle of constant field scaling and examine its effect on device characteristics.	CO3-Ana	(6)
14.	(a)	Discuss the comparison of circuit families	CO4 -U	(16)
		Or		
	(b)	(i) Discuss the domino logic with neat diagram.	CO4- U	(8)
		(ii) Explain the problem of metastability with neat diagrams and expressions.	CO4-U	(8)
15.	(a)	Describe the scan based approaches and built in self-test to design for testability in detail.	CO5- U	(16)
		Or		
	(b)	(i) Discuss the Silicon debug principles in detail	CO5-U	(8)
		(ii) Explain the Boundary scans techniques.	CO5-U	(8)