Reg. No. : | | | | | | | | | | |

Question Paper Code: 39403

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2019

Elective

Electronics and Communication Engineering

01UEC903 - COMPUTER ARCHITECTURE AND ORGANIZATION

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. List out the register level circuit components.
2. Differentiate direct and indirect addressing mode.
3. Compare spatial expansion and temporal expansion.
4. Discuss the principle behind the Booth's multiplier.
5. What is microprogramming?
6. What is Write-After-Write (WAW) hazard?
7. Compare sequential access and random access memories.
8. Define Hit ratio.
9. List out the limitations of the programmed I/O data transfer method.
10. How many 128 * 4 RAM memory chips are required to construct RAM memory system of 1 *Kbytes*?

PART - B (5 x 16 = 80 Marks)

11. (a) Explain zero, one, two and three addressing instructions with example. (16)

Or

(b) Explain the operation of each functional unit in the computer system with suitable diagram. (16)

12. (a) With a neat block diagram explain in detail about CPU-coprocessor interfacing. (16)

Or

(b) With a neat sketch, explain in detail about logic design for fast adders. (16)

13. (a) Explain the design of micro-programmed control unit for the two's complement multiplier with a diagram. (16)

Or

(b) (i) Describe the design details of pipelined processing. (10)

(ii) Write short notes on Nano programming. (6)

14. (a) (i) Design the following RAM using N x w bit IC RAM.

(1) N x 4w bit RAM

(2) 4N x w bit RAM (10)

(ii) Write short notes on optical memories. (6)

Or

(b) Explain the concepts of memory hierarchies. (16)

15. (a) With a diagram explain static and dynamic redundancy for designing fault tolerant system. (16)

Or

(b) (i) Explain the design aspects of vectored interrupts. (10)

(ii) Compare RISC and CISC processor. (6)