Reg. No. : | | | | | | | | | | |

Question Paper Code: 53504

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2019

Third Semester

Electronics and Instrumentation Engineering

15UEI304 - DIGITAL ELECTRONICS

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. Which of the following is minimum error code?

   (a) Octal code (b) Grey code
   (c) Binary code (d) Excess 3 code

2. Which of the following expressions is in the sum-of-products (SOP) form?

   (a) *AB + CD* (b) *AB(CD)* (c) *(A + B)(C + D)* (d) *(A)B(CD)*

3. A NAND gate is called a universal logic element because

   (a) it is used by everybody
   (b) any logic function can be realized by NAND gates alone
   (c) all the minization techniques are applicable for optimum NAND gate realization
   (d) many digital computers use NAND gates

4. How many bits are required to store one BCD digit?

   (a) 1 (b) 2 (c) 3 (d) 4

5. For which of the following flip-flops, the output is clearly defined for all combinations of two inputs

   (a) Q type flip-flop (b) R-S flip-lop (c) J-K flip-lop (d) D flip-flop

6. How many flip flops are required to construct a decade counter?

(a) 10 (b) 8 (c) 5 (d) 4

7. Table that is not a part of asynchronous analysis procedure.

(a) transition table (b) state table
(c) flow table (d) excitation table

8. Race in which stable state depends on order is called

(a) critical race (b) identical race
(c) non critical race (d) defined race

9. Which of the following memories uses one transistor and one capacitor as basic memory unit

(a) SRAM (b) DRAM (c) Both (a) and (b) (d) none

10. In a read-only memory information can be stored

(a) at the time of fabrication
(b) by the user only once during its life time
(c) by the user a number of times
(d) in any of the above ways depending upon the type of memory

PART - B (5 x 2 = 10 Marks)

11. Define De-morgan's theorem.

12. Draw $Y = A + BCD'$ using NAND only.

13. Write down the characteristic equation for JK flip flop.

14. Compare static and dynamic hazards.

15. What is programmable logic array? How it differs from ROM?

PART - C (5 x 16 = 80 Marks)

16. (a) Minimize the given switching function using Quine-Mcclusky method.
f(x1, x2, x3, x4)= Σ(0, 5, 7, 8, 9, 10, 11, 14, 15). (16)

Or

(b) Simplify the following expression using K-map

(i) $Y = \sum_m (7, 9, 10, 11, 12, 13, 14, 15)$

(ii) $Y = m_1 + m_5 + m_{10} + m_{11} + m_{12} + m_{13} + m_{15}$ (16)

17. (a) Design a BCD adder and explain its working with necessary logic diagram. (16)

Or

(b) (i) Give the CMOS logic circuit for NOR gate and explain its operation. (8)

(ii) Explain the TTL circuit output connections. (8)

18. (a) Design and explain a ring counters with suitable example. (16)

Or

(b) Explain the operation of universal shift register with logic diagram. (16)

19. (a) (i) Define races and explain its types. (8)

(ii) Explain how hazards that occur in asynchronous circuits (8)

Or

(b) What are hazards? When does the hazard occur in combinational circuits and quote an example? Name the types of hazards and how they are avoided. (16)

20. (a) Explain with neat diagrams a RAM architecture. (16)

Or

(b) (i) Draw the block diagram of a PLA and explain its IC 7575-PLA. (16)

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