Reg. No. : | | | | | | | | | | |

Question Paper Code: 43506

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2019

Third Semester

Electronics and Instrumentation Engineering

14UEI306 – DIGITAL ELECTRONICS

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. How is a *J-K* flip-flop made to toggle?

   (a) $J = 0, K = 0$ (b) $J = 1, K = 0$ (c) $J = 0, K = 1$ (d) $J = 1, K = 1$

2. Which of the following is correct for a gated D flip-flop?

   (a) The output toggles if one of the inputs is held high
   (b) Only one of the inputs can be high at a time
   (c) The output complement follows the input when enabled
   (d) *Q* output follows the input *D* when the enable is high

3. A comparator is a special combinational circuit designed primarily to compare the relative magnitude of _____ numbers .

   (a) two decimal (b) three decimal (c) two binary (d) three binary

4. The systematic reduction of logic circuits is accomplished by

   (a) using Boolean algebra (b) symbolic reduction
   (c) TTL logic (d) using a truth table

5. How is a J-K flip-flop made to toggle?

(a) J = 0, K = 0 (b) J = 1, K = 0 (c) J = 0, K = 1 (d) J = 1, K = 1

6. What is a major disadvantage of RAM?

(a) Its access speed is too slow (b) Its matrix size is too big
(c) It is volatile (d) High power consumption

7. Race in which stable state depends on order is called

(a) critical race (b) identical race
(c) non critical race (d) defined race

8. In design procedure of asynchronous circuit flow table is

(a) increased to max states (b) reduced to min states
(c) changed (d) remain same

9. PAL consists of a programmable ____ array and a fixed _____ array with output logic.

(a) NAND and NOR (b) AND and NOR
(c) NAND and OR (d) AND and OR

10. _____ is the minimum time required to maintain a constant voltage levels at the excitation inputs of the flip-flop device.

(a) Rise time (b) Fall time
(c) Setup time (d) None of these

PART - B (5 x 2 = 10 Marks)

11. Simplify: $A + AB + \overline{A} + B$.

12. Write the truth table of a 4:1 multiplexer.

13. Define synchronous counter.

14. Define primitive flow table.

15. What is meant by PLA?

PART - C (5 x 16 = 80 Marks)

16. (a) Simplify the Boolean function using tabulation method.
Y (A, B, C, D)= ∑ m (1, 2, 3, 5, 9, 12, 14, 15)+∑ D (4, 8, 11). (16)

Or

(b) Find the minimal sum of products for the Boolean expression $f(w,x,y,z) = \sum (1,3,4,5,9,10,11) + \sum d(6,8)$ using tabulation method. (16)

17. (a) (i) Compare the characteristics of different Logic families. (8)

(ii) Design a 4-bit Parallel Adder/Subtractor using logic gates. (8)

Or

(b) Design BCD adder and explain its working with necessary circuits. (16)

18. (a) (i) How will you convert a D flip flop into JK flip flop? (8)

(ii) Sketch a 4-bit serial in serial out shift register and draw its waveforms. (8)

Or

(b) Explain the operation universal shift register with logic diagram. (16)

19. (a) Explain with neat diagram the different hazards and the way to eliminate them. (16)

Or

(b) Explain the different methods of state assignment. (16)

20. (a) (i) With a neat sketch, explain the block diagram of PLA. (8)

(ii) Discuss in detail about EPROM and EEPROM. (8)

Or

(b) Explain with neat diagrams a RAM architecture. (16)

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