Reg. No. : | | | | | | | | | | |

Question Paper Code: 33506

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2019

Third Semester

Electronics and Instrumentation Engineering

01UEI306 – DIGITAL ELECTRONICS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. State De Morgan's theorem.
2. List out the advantages and disadvantages of K-map method.
3. Define half adder and full adder.
4. Design a half -subtractor using basic gates.
5. Give the applications of flip flop.
6. What is a shift register? And mention its types.
7. Define race condition.
8. Define hazards.
9. Compare PROM and EPROM.
10. Draw the basic configuration of PLA.

PART - B (5 x 16 = 80 Marks)

11. (a) Compute the minimized Boolean expression using K-map
F = A'BC'D'+A'BC'D+ ABC'D'+ AB'C'D+ A'B'CD' (16)

Or

(b) Given Y (A, B, C, D) = ∏M (0, 1, 3, 5, 6, 7, 10, 14, 15), draw the K-map and obtain the simplified expression and realize using basic gates (16)

12. (a) Design a combinational logic using a suitable multiplexer to realize the Boolean expression: F = AD'+B'C+BC'D. (16)

Or

(b) Design a BCD to Excess-3 converter using truth table and k-map simplification. (16)

13. (a) Design a mod-7 synchronous binary counter using JK flip-flops. (16)

Or

(b) Design a 3-bit synchronous counter which counts in the sequence 000, 001, 011, 010,100, 110, (repeat) 000 using D flip flop. (16)

14. (a) Design a asynchronous sequential circuit specified by the following flow table. (16)

	00	01	10	10
A	A.O	A.O	A.O	B.0
B	A,O	A.O	B.1	B.1

Or

(b) Design a asynchronous circuits that will produce output only the first pulse received and ignore if any other pulses. (16)

15. (a) Implement the BCD to XS3 code conversion using ROM. (16)

Or

(b) Implement the following function using PLA. F_1 (x, y, z) = ∑m (1, 2, 4, 6); F_2 (x, y, z) = ∑m (0, 1, 6, 7); F_3 (x, y, z) =∑m (2, 6). (16)