Reg. No. : | | | | | | | | | | |

Question Paper Code: 46503

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2019

Sixth Semester

Electronics and Instrumentation Engineering

14UEI603 - REAL TIME EMBEDDED SYSTEMS ARCHITECTURE

(Regulation 2014)

Duration: Three hours   Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The 8051 has _____ 16-bit counter/timers.

    (a) 1   (b) 2   (c) 3   (d) 4

2. Match the following:

    1) TCON   (i)   contains status information

    2) SBUF   (ii)   timer/counter control register.

    3) TMOD   (iii) idle bit, power down bit

    4) PSW   (iv)   serial data buffer for Tx and Rx.

    5) PCON   (v)   timer/ counter modes of operation

    (a) 1->ii, 2->iv, 3->v, 4->i, 5->iii   (b) 1->i,   2->v,   3->iv,   4->iii,   5->ii
    (c) 1->v, 2->iii, 3->ii, 4->iv, 5->i   (d) 1->iii, 2->ii, 3->i, 4->v, 5->iv

3. What is the order decided by a processor or the CPU of a controller to execute an instruction?

    (a) decode, fetch, execute   (b) execute, fetch, decode

    (c) fetch, execute, decode   (d) fetch, decode, execute

4. Abbreviate CISC and RISC

   (a) Complete Instruction Set Computer, Reduced Instruction Set Computer

   (b) Complex Instruction Set Computer, Reduced Instruction Set Computer

   (c) Complex Instruction Set Computer, Reliable Instruction Set Computer

   (d) Complete Instruction Set Computer, Reliable Instruction Set Computer

5. The Width of a processor's data path is measured in bits. Which of the following are common data paths?

   (a) 8 bits   (b) 12 bits   (c) 16 bits   (d) 32 bits

6. What are the essential tight constraint/s related to the design metrics of an embedded system?

   (a) Ability to fit on a single chip
   (b) Low power consumption
   (c) Fast data processing for real-time operations
   (d) All the above

7. What is the directional nature of two active wires SDA and SCL usually adopted in I2C Bus for carrying the information between the devices.

   (a) Uni-directional   (b) Bi-directional
   (c) Multi-directional   (d) None of these

8. The DMA transfers are performed by a control circuit called as

   (a) Device interface   (b) DMA controller
   (c) Data controller   (d) Over looker

9. Two partitions must be insulated to prevent operations on one half from affecting other, such floating-point operations are called

   (a) Single-instruction operation   (b) Vector operation
   (c) Paired single operations   (d) Fetch operation

10. Which of these is a digital input device?

   (a) pressure sensor   (b) servo
   (c) button   (d) potentiometer

PART - B (5 x 2 = 10 Marks)

11. Port 0 be used as input output port? Justify.

12. Write a program to toggle all bits of P1 every 200ms.

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13. Mention the typical characteristics of an embedded system.

14. What do you meant by bus arbitration?

15. What is the difference between mutexes and semaphores?

PART - C (5 x 16 = 80 Marks)

16. (b) Write an 8051 Program to send the two messages "Normal Speed" and "High Speed" to the serial port. Assuming that SW is connected to pin P2.0, monitor its status and set the baud rate as follows:

      SW = 0, 28,800 baud rate

      SW = 1, 56K baud rate

   Assume that XTAL = 11.0592 MHz for both cases.   (16)

Or

   (b) Describe the interrupt structure of 8051 microcontroller with neat diagram.   (16)

17. (a) Write a program to interface liquid crystal display with 8051 microcontroller and display the message "Success".   (16)

Or

   (b) Describe with a neat diagram the stepper motor control using microcontroller.   (16)

18. (a) Explain in detail about the design process of automatic chocolate vending machine with suitable diagram.   (16)

Or

   (b) Describe in detail about the types of memory used in embedded system.   (16)

19. (a) With suitable diagram, explain in detail about the parallel communication using ISA, PCI and PCI/X buses.   (16)

Or

   (b) Explain in detail about ISA bus.   (16)

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20. (a) Discuss in detail about the different concepts of semaphores with necessary diagram. (16)

Or

(b) Explain in detail about the interrupt latency and deadline. (16)

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