A **Reg. No. :** | | | | | | | | | | |

Question Paper Code: 59501

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2019

Elective

Electronics and Instrumentation Engineering

15UEI901– VLSI SYSTEM DESIGN

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. Which technology has photo-electronic properties? CO1-R

   (a) GaAs (b) BiCMOs (c) CMOS (d) nMOS

2. Approximately how many numbers of transistors per chip is available in MSI CO1-R

   (a) 10-100 (b) 100-1,000 (c) 1,000-10,000 (d) > 10,000

3. In the design rules the implant layer has CO2-R

   (a) 2λ x 2λ (b) 4λ x 4λ (c) 6λ x 6λ (d) 8λ x 8λ

4. The ratio of pull-up to pull-down for an inverter directly driven by an inverter is CO2-R

   (a) 2/1 (b) 3/2 (c) 8/1 (d) 4/1

5. Precharge low circuits are slower to pull up than precharge high circuits are to pull down. This statement is _____. CO3-R

   (a) True (b) False (c) based on logic (d) based on clock

6. Barrel shifter requires _____ control lines. CO3-R

   (a) 2N (b) N^2 (c) $2N^2$ (d) N

7. The line connecting OR Plane and AND Plane in an NMOS PLA is called CO4-R

   (a) Product line (b) Sum line (c) Connector (d) Interconnection

8. PLA contains CO4-R

(a) AND and OR arrays (b) NAND and OR arrays

(c) NOT and AND arrays (d) NOR and OR arrays

9. _____ is used for local storage of temporary data, visible only inside a process. CO5-R

(a) Signal (b) Variable (c) Constant (d) Entity

10. The full form of VHDL is CO5-R

a)Very High Descriptive Language

(b)Very High Definition Language

(c)Variable Definition Language

(d) None of the Mentioned

PART – B (5 x 2= 10Marks)

11. Define body effect. CO1-U

12. Mention techniques to reduce switching activity. CO2-U

13. Define Contamination delay. CO3-U

14. List the steps used for design flow in VLSI. CO4-U

15. What is subprogram? CO5-R

PART – C (5 x 16= 80Marks)

16. (a) Discuss in detail about the modes of operation of MOS transistor with necessary equations. CO1- U (16)

Or

(b) (i) Derive the NMOS transistor current equations in all regions. CO1- U (8)

(ii) Describe the Enhancement mode operation of MOS transistor. CO1- U (8)

17. (a) Determine the pull up to pull-down ratio of nMOS Inverter driven by another nMOS Inverter. CO2 -U (16)

Or

(b) (i) Verify the pull up to pull-down ratio of nMOS Inverter driven by nMOS Inverter through pass transistor is 8:1. CO2 -App (8)

(ii) Draw the stick diagram and mask diagram of the nMOS Inverter and CMOS Inverter. CO2- App (8)

18.	(a)	(i)Design an 4 x 4 Barrel Shifter and explain its operation.	CO3- App	(16)
		(ii)Design a 3 input Tally Circuit.	CO3-App	
		Or		
	(b)	(i)Design a 4 x 1 Multiplexer using CMOS static pull up device.	CO3- App	(16)
		(ii) Sketch a clocked precharged – high, 2 input NMOS NOR Gate	CO3-App	
19.	(a)	What is programmable logic devices? Explain the different types of PLD in detail	CO4- App	(16)
		Or		
	(b)	Design and sketch the stick diagram of a NMOS NAND-NAND PLA realization of the product lines with three output lines. $P_0 = \overline{I_0}\,\overline{I_1}$ $P_1 = \overline{I_0} I_1$ $P_2 = I_0 I_1 \overline{I_2}$ $P_3 = I_0 I_2$ $Y_0 = P_1$ $Y_1 = P_0 + P_2 + P_3$ $Y_2 = P_1 + P_2$	CO4- App	(16)
20.	(a)	Explain in detail about the design procedure of RTL.	CO5- U	(16)
		Or		
	(b)	(i)Write a testbench VHDL program for NAND gate.	CO5 -App	(8)
		(ii)Draw the diagram of down counter and write the VHDL program.	CO5- App	(8)

59501