Reg. No. : | | | | | | | | | | |

Question Paper Code: 43203

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2019

Third Semester

Computer Science and Engineering

14UCS303 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

(Smith chart may be permitted)

PART A - (10 x 1 = 10 Marks)

1. Which of the following would take less execution time?

   (a) Memory –Memory instruction (b) Register – Register instruction
   (c) Register – memory instruction (d) Memory – register instruction

2. Add 20(R0,R1) , R2 is an example of

   (a) Indirect addressing (b) Absolute addressing
   (c) Indexed Addressing (d) Direct Addressing

3. Arithmetic Logic Unit (ALU) is used to perform

   (a) addition (b) left shift (c) right shift (d) all of these

4. The number of bits for exponent field in double precision floating point number is

   (a) 8 bits (b) 11 bits (c) 20 bits (d) 23 bits

5. The throughput of an ideal pipeline with *k* stages is _____ instruction/clock cycle

   (a) *k* (b) *k*-1 (c) 1 (d) 2

6. Which of the following MIPS instruction takes more execution time?

(a) Load word(lw) (b) Store word(sw) (c) R-format(add) (d) Branch(beq)

7. Multithreading an interactive program will increase responsiveness to the user by

(a) continuing to run even if a part of it is blocked
(b) waiting for one part to finish before the other begins
(c) asking the user to decide the order of multithreading
(d) None of these

8. In a multithreaded environment _____

(a) Each thread is allocated with new memory from main memory
(b) Main thread terminates after the termination of child threads
(c) Every process can have only one thread
(d) No termination

9. The signal sent to the device from the processor to the device after receiving an Interrupt is

(a) Interrupt-acknowledge (b) Return signal
(c) Service signal (d) Permission signal

10. The extra time needed to bring the data into memory in case of a miss is called as

(a) Delay (b) Propagation time (c) Miss penalty (d) Data latency

PART - B (5 x 2 = 10 Marks)

11. Why the data bus is bidirectional while the address bus is unidirectional?

12. What is the purpose of guard bits in floating point operations?

13. What is the role of multiplexer in Single bus organization?

14. Provide Flynn's classification of parallel computers.

15. Find the average memory access time for a processor with a 1 *ns* clock cycle time, a miss penalty of 20 clock cycles, a miss rate of 0.05 misses per instruction and cache access time of 1 clock cycle.

PART - C (5 x 16 = 80 Marks)

16. (a) (i) With a neat diagram, explain the basic operational steps needed to execute the instruction Add LOCA, R0. (8)

(ii) How would you measure and report the performance of a computer? (8)

Or

(b) (i) Describe the different classes of Instruction format with examples. (12)

(ii) Registers *R*1 and *R*2 of a computer contain the decimal values 1200 and 2400 respectively. What is the effective address of the memory operand in each of the following instructions?

Load 20(*R*1), *R*5

Add –(*R*2), *R*5 (4)

17. (a) (i) Design a fast adder by deriving generate and propagate functions. (8)

(ii) Explain the steps in Booth algorithm. (8)

Or

(b) Derive and explain an algorithm for adding and subtracting two floating point binary numbers. (16)

18. (a) Give a typical single bus organization connecting the various parts of the CPU and show how the instruction ADD *R*0, *R*1,(*R*2) gets executed. Assume that the instruction is a one word instruction and *R*0, *R*1 are source operands and (*R*2) is the destination operand. (16)

Or

(b) Discuss the various hazards that might arise in a pipeline. What are the remedies commonly adopted to overcome / minimize these hazards? (16)

19. (a) Discuss about the hardware and Compiler approaches for instruction level parallelism. (16)

Or

(b) Explain Flynn's classification of computers. (16)

20. (a) What is virtual memory? Explain the address translation scheme. (16)

Or

(b) (i) What is DMA? What are the steps in DMA transfer? (8)

(ii) Explain the working of a DMA controller with a diagram. (8)