Reg. No. : | | | | | | | | | | |

Question Paper Code: 42207

B.E. / B.Tech. DEGREE EXAMINATION, NOV 2019

Second Semester

Computer Science and Engineering

14UCS207 – DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 1 = 10 Marks)

1. The output of an AND gate is LOW _____.
   (a) when any input is LOW (b) when any input is HIGH
   (c) when all inputs are HIGH (d) all the time
2. When used with an IC, what does the term "QUAD" indicate?
   (a) 4 circuits (b) 2 circuits (c) 8 circuits (d) 6 circuits
3. Which of the following expressions is in the sum-of-products (SOP) form?
   (a) AB + CD (b) AB(CD) (c) (A + B)(C + D) (d) (A)B(CD)
4. The systematic reduction of logic circuits is accomplished by:
   (a) symbolic reduction (b) using Boolean algebra
   (c) TTL logic (d) using a truth table
5. A demultiplexer is used to ----------
   (a) perform arithmetic division
   (b) select data from several inputs and route it to a single output
   (c) steer the data from a single input to one of the many outputs
   (d) perform parity checking

6. An EPROM----------

(a) is of random – access type (b) is non – volatile

(c) is programmable (d) has all the above requirements

7. The basic shift register operations are

(a) serial in serial out (b) serial in parallel out

(c) parallel in serial out (d) all of the above

8. For which of the following flip-flop the output clearly defined for all combinations of two inputs?

(a) Q type flip-flop (b) R S type flip-flop

(c) J K flip-flop (d) T flip-flop

9. Combinations that are not listed for input variables are

(a) overflows (b) carry (c) dont cares (d) zero bits

10. If two systems have different codes then circuit inserted between them is

(a) sequential circuit (b) combinational circuit

(c) combinational sequence circuit (d) conversion circuit

PART - B (5 x 2 = 10 Marks)

11. Show that the dual of the exclusive-OR is equal to its complement

12. Explain the design procedure for combinational circuits.

13. Give the applications of Demultiplexer.

14. Justify the need for edge triggering.

15. What is a Hazard in Digital circuit?

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Find the Minimized logic function using K-Maps and Realize sing NAND and NOR gate. $F(A,B,C,D)= \sum m(1,3,5,8,9,11,15) + d(2,13)$ (8)

(ii) Show that if all the gate in a two-level OR-AND gate network are replaced by NOR gate, the output function does not change. (8)

Or

(b) How would you express the Boolean function using K-map and draw the logic diagram F(w,x,y,z)= $\sum m(0,1,2,4,5,6,8,9,12,13,14)$ (16)

17. (a) (i) Analyze the function of Binary multiplier with neat diagram. (8)

(ii) Develop a Full adder using decoder. (8)

Or

(b) Combinational logic circuit has two inputs (a,b) and four outputs (w,x,y,z). The outputs represent a binary number whose value equals the square of input. For example, if ab=10, then wxyz=0100. Design the circuit and show the logic diagram. (16)

18. (a) (i) Implement the following Boolean function with a 4:1 multiplexer and external gates.

$F(A, B, C, D)=\sum(1, 3, 4, 11, 12, 13, 14, 15)$. (8)

(ii) Using a decoder and external gates, design the combinational circuits defined by the following three Boolean functions:

$F1=x'y'z' +xz +yz$

$F2=xy'z' + x'y$

$F3=x'y'z + xy$ (8)

Or

(b) Design a BCD to Excess 3 code converter using PROM. (16)

19. (a) A sequential circuit has two flip flops (A and B), two inputs (x and y) and an output (Z). The flip flop input functions and the circuit output function are as follows.

JA = XB + y'B KA = xy'B'

JB = xA' KB = xy' + A

Z = xyA + x'y'B

Obtain the logic diagram; sate table, state diagram and state equations. (16)

Or

(b) Define encoder. Explain priority encoder with an example. (16)

20. (a) Design an asynchronous sequential circuit with two inputs *X* and *Y* and with one output *Z*. Whenever *Y* is 1, input *X* is transferred to *Z*. When *Y* is 0, the output does not change for any change in *X*. Use D- Flip flop for implementation of the circuit. (16)

Or

(b) With suitable example explain Race Free State assignment. (16)