Reg. No. : | | | | | | | | | | |

Question Paper Code: 32271

M.E. DEGREE EXAMINATION, MAY 2016

Second Semester

VLSI Design

01PVL201 - ANALYSIS AND DESIGN OF ANALOG INTEGRATED CIRCUITS

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Draw the Small Signal Model of BJT.
2. What is meant by "Weak Inversion" in MOS transistors?
3. Draw the emitter follower circuit and mention the advantage of this configuration.
4. What is the necessary condition for biasing?
5. Define Slew rate and justify its importance in OP AMP.
6. Draw an ac schematic circuit of a common emitter amplifier and its equivalent circuit using Miller approximation.
7. Explain the roll of phase detector in Multiplier cell.
8. Draw the block diagram of a Phase Locked Loop system.
9. Draw a simple current mirror circuit using n-channel MOSFETs.
10. What are the advantages of class AB output stage?

PART - B (5 x 14 = 70 Marks)

11. (a) (i) Explain the depletion region of a PN junction. (4)

(ii) Draw the basic small signal model of the bipolar transistor and derive the collector–base resistance and the collector–base capacitance. (10)

Or

(b) (i) Draw the Small Signal model of MOSFET and explain in detail. (10)

(ii) Explain briefly the capacitive effects present in MOSFET. (4)

12. (a) Explain the band gap reference bias circuits in CMOS technology to get temperature insensitive voltage references. (14)

Or

(b) (i) Discuss about the differential amplifier with active load using FET. (10)

(ii) Draw the band gap reference circuit and explain. (4)

13. (a) (i) Discuss and analyze the slew rate model of OP amp. (10)

(ii) Write notes on OP AMP noise. (4)

Or

(b) Explain the dominant-pole approximation of a multistage amplifier and derive the 3 dB frequency. (14)

14. (a) Explain the DC analysis of a Gilbert Multiplier Cell its use as an analog multiplier. (14)

Or

(b) Explain in detail about the closed loop analysis of PLL. (14)

15. (a) Explain the large signal analysis and small signal analysis of a differential pair with Current mirror load. (14)

Or

(b) Explain the MOS Active – Cascade Operational Amplifiers. (14)

PART - C (1 x 10 = 10 Marks)

16. (a) Sketch the cross section of a bipolar transistor and derive the equations to obtain the large signal characteristics. (10)

Or

(b) Explain the CMOS Class AB output stages with a neat diagram. (10)