Reg. No. : | | | | | | | | | | |

Question Paper Code: 52974

M.E. DEGREE EXAMINATION, JUNE 2016

Elective

VLSI Design

15PVL513 – DESIGNING WITH CPLDS AND FPGAS

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 20 = 100 Marks)

1. (a) (i) Explain in detail about Shannon's expansion theorem with relevant equations. (10)

(ii) Design 8:1 multiplexer by using 4:1 multiplexer. (10)

Or

(b) (i) With an example give detailed description about static and dynamic hazard and how it can be avoided. (10)

(ii) Realize a hazard free circuit for following Boolean function:
$Z=a'd'+ab'+ac'+bc'$. (10)

2. (a) Design a BCD to Excess 3 code converter as a Mealy sequential circuit. (20)

Or

(b) Design a serial binary adder as a Moore sequential circuit. (20)

3. (a) Design a fundamental –mode asynchronous sequential network meeting the following requirements:

(i) There are two inputs x1 and x2 and a single output z.

(ii) The inputs and x1 and x2 never change simultaneously.

(iii) The output is always to be 0 when x1=0, independent of the value of x2.

(iv) The output is to become 1 if x2 changes while x1=1 and is to remain 1 until x1 becomes 0 again (20)

Or

(b) Draw the architecture of CPLD and explain each block in detail. (20)

4. (a) (i) Realize the following functions using PLA:

$F0=\sum m(0, 1, 4, 6)$

$F1=\sum m(2, 3, 4, 6, 7)$

$F2=\sum m(0, 1, 2, 6)$

$F3=\sum m(2, 3, 5, 6, 7)$ (10)

(ii) Realize the following functions with suitable PAL:

$F1=xy'+xz+y'z+x'yz'$

$F2=z+x'y'$

$F3=xy'+xz$ (10)

Or

(b) Design a parallel binary multiplier using ASM. (20)

5. (a) With neat sketch explain in detail about architecture of FPGA. (20)

Or

(b) Design mod-6 counter using Xilinx 3000 series FPGA. (20)