Reg. No. : | | | | | | | | | | |

Question Paper Code: 52973

M.E. DEGREE EXAMINATION, JUNE 2016

Elective

VLSI Design

15PVL506 - THREE DIMENSIONAL IC

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 20 = 100 Marks)

1. (a) (i) Summarize the role of importance and the degradation caused by interconnect to IC industry. (15)

(ii) Using flow diagram draw the evolution of logic styles. (5)

Or

(b) Discuss in detail about the opportunities and challenges for three dimensional integration technologies. (20)

2. (a) (i) With the help of process steps describe the fabrication of 3D ICs with through silicon vias. (10)

(ii) Illustrate the electrical model of an TSV using RLC model to describe the power and speed of an 3D circuit. (10)

Or

(b) (i) Compare and contrast the capacitively coupled and inductively coupled 3D ICs. (10)

(ii) Evaluate the different fabrication techniques for stacked 3D ICs. (10)

3. (a) Explain in detail about the multi-step and multi-objective floor planning for 3D ICs. (20)

Or

(b) Investigate the different techniques addressed to route in third dimension of integrated circuits. (20)

4. (a) Consider an inter plane two-terminal net connecting two circuits located on different physical planes including one inter plane via. Using delay model explain the variation in delay with via location and conclude the optimum via location for different impedance characteristics of the interconnect segments. (20)

Or

(b) Discuss about near optimal heuristics for placing vias in interconnect trees in 3D integrated circuits and the via placement algorithms for interconnect trees. (20)

5. (a) (i) Discuss in detail about the three dimensional microprocessor logic blocks and cache memories. (15)

(ii) Recall the topologies and terminologies used for 3D ICs and 3D NoCs. (5)

Or

(b) With the help of diagrams explain three dimensional FPGAs and the design aids for 3D FPGAs. (20)

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