Reg. No. : | | | | | | | | | | |

Question Paper Code: 52971

M.E. DEGREE EXAMINATION, JUNE 2016

Elective

VLSI Design

15PVL503 - VLSI SIGNAL PROCESING

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 20 = 100 Marks)

1. (a) Explain the various representations of DSP algorithms with an example. (20)

Or

(b) With your own example explain the largest path matrix algorithm to find the iteration bound. (20)

2. (a) Define retiming and explain the properties of retiming. (20)

Or

(b) Define unfolding and describe in detail about any two applications of unfolding. (20)

3. (a) Derive a 2 x 2 convolution algorithm using the modified Cook-Toom algorithm with $\beta_0 = 0$ and $\beta_1 = -1$. (20)

Or

(b) With an example explain how speedup is achieved in IIR filter by combining both pipelining and parallel processing. (20)

4. (a) (i) Write about scaling operation and round of noise. (10)

(ii) Describe the computation of scaling and round of noise. (10)

Or

(b) (i) Compute the CSD representation of the input number 1.01110011. (5)

(ii) Explain CSD multiplication using Horner's rule. (15)

5. (a) What is sub expression elimination? Apply sub expression elimination to the following polynomials.

(i) $X^{22}+X^{19}+X^{14}+X^{7}+X$

(ii) $X^{29}+X^{23}+X^{20}+X^{15}+X^{9}+X$

(iii) $X^{23}+X^{17}+X^{18}+X^{5}+X^{4}+X$

Determine the number of multiplications required to evaluate the polynomials both before and after sub expression elimination is applied. (20)

Or

(b) (i) Explain in detail about the wave pipelining. (10)

(ii) Write short notes on single phase clocking and two phase clocking. (10)

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