Reg. No. : | | | | | | | | | | |

Question Paper Code: 41362

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2016

Third Semester

Instrumentation and Control Engineering

14UIC302 - DIGITAL LOGIC CIRCUITS AND DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. $(EF)_{16}$ in octal number system

   (a) 257 (b) 736 (c) 357 (d) 737

2. What is A.1

   (a) 1 (b) A’ (c) 0 (d) A+A

3. An Encoder has

   (a) 2n inputs (b) n^2 inputs (c) 2^n inputs (d) n+2 inputs

4. Which is per mentally fused?

   (a) PLA (b) PAL (c) PROM (d) EPROM

5. When S and R is clubbed together in SR flip-flop then it is called as

   (a) JK flip-flop (b) T flip-flop (c) D flip-flop (d) SR Latch

6. Shift registers have

   (a) uneven clock pulse (b) even clock pulse
   (c) no clock pulse (d) none of these

7. The asynchronous circuit depends upon

(a) change in input (b) change in output
(c) change in time (d) change in ripples of clock pulse

8. The present status of asynchronous circuit is also called as

(a) excitation variables (b) input variables
(c) primary variables (d) secondary variables

9. I^2L operation is similar to

(a) TTL (b) RTL (c) ECL (d) CMOS

10. Propagation delay is decreased in

(a) I^2L (b) TTL (c) Schotty diode (d) ECL

PART - B (5 x 2 = 10 Marks)

11. Get the 10's complement for 63 – 36.

12. Differentiate between PROM and EPROM.

13. What is shift registers?

14. Differentiate between asynchronous sequential circuit and synchronous sequential circuit.

15. List the configuration of TTL.

PART - C (5 x 16 = 80 Marks)

16. (a) Estimate the prime implicants for the following expression $F = \Sigma$ (1, 4, 6, 7, 8, 9, 10, 11, 15). Use tabulation method. (16)

Or

(b) (i) Plot the expression F (ABCD) = Σ (2, 3, 6, 7, 10, 11, 15, 26, 27, 30, 31, 18, 23) on K-map. Get a simplified expression. Use suitable don't care conditions such that the simplified expression is F = D. (10)

(ii) Get the simplified expression F (wxyz) = Σ (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14). Use K-map simplification. (6)

17. (a) (i) Assuming there are 3 outputs (O1, O2, O3) operating for 3 inputs. If the 1st input is available the outputs become unstable. The second and the third inputs are available or any one second or third input is available then the output O1 exits. If the second input is available then all the three outputs are existing. Design a combination circuit. (8)

(ii) Design a BCD to Excess – 3 code converter. (8)

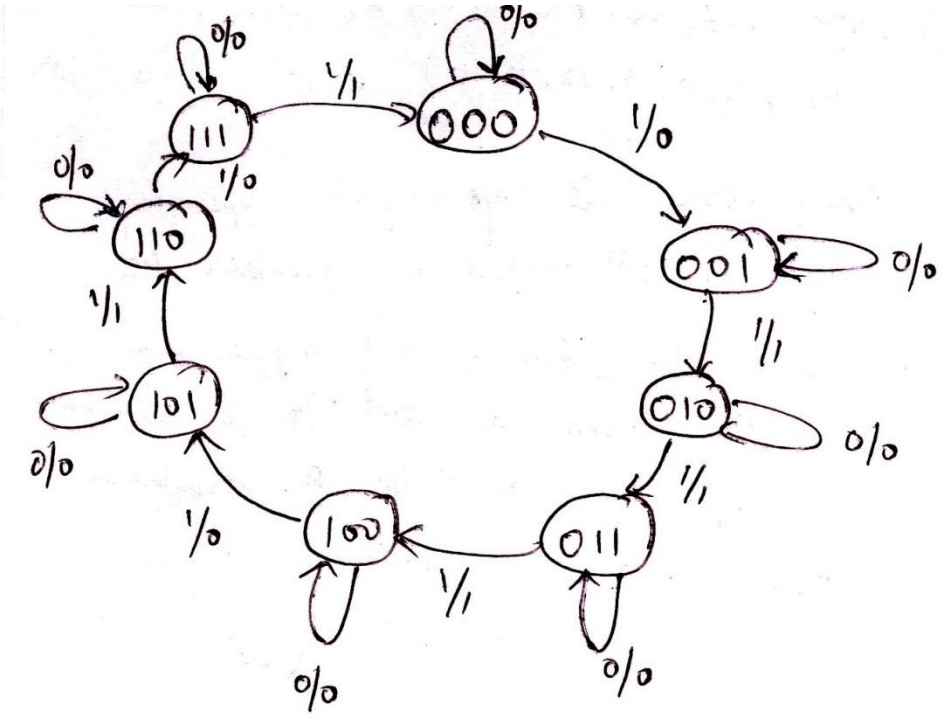
Or

(b) (i) Construct a PAL, Given the function F (ABCD) = Σ (0, 3, 5, 7, 9, 13) and d Σ (1, 6, 12). (6)

(ii) Construct a PLA, Given the function F (ABCD) = Σ (0, 3, 5, 7, 9, 13) and d Σ (10, 14). (6)

(iii) Compare PAL and PLA. (4)

18. (a) Design a circuit as indicated by the state diagram. Use JK flip-flop. (16)



Or

(b) Design a BCD up-counter. Use T flip-flop. (16)

19. (a) Design a circuit given two input gate (G) Data (D) output (Q).

(i) If the binary information is present at D input this transfers to the Q output when G = 1

(ii) Q output will follow the D input as long as G = 1

(iii) When G goes to 0, the information that was present at the D input at the time, the transition occurred is retained at Q output (16)

Or

(b) (i) What is the procedure for obtaining the transition table form the circuit diagram of an asynchronous sequential circuit? (8)

(ii) Discuss in detail the race conditions. (8)

20. (a) Discuss in detail metal oxide semiconductor and hence explain how MOS is differentiated from CMOS? (16)

Or

(b) (i) Write a VHDL program for mod-6 up counter. (6)

(ii) Write a VHDL program for full adder using half adder. (10)