Reg. No. : | | | | | | | | | | |

Question Paper Code: 41336

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2016

Third Semester

Electrical and Electronics Engineering

14UEE306 - DIGITAL LOGIC CIRCUITS

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. How many binary numbers are created with 8 bits?

   (a) 128 (b) 256 (c) 64 (d) 32

2. 8421 code is

   (a) weighted code (b) self complemented code
   (c) un weighted code (d) alphanumeric code

3. How many inputs and outputs does a full adder have?

   (a) two inputs, two output (b) two inputs, three outputs
   (c) three inputs, two output (d) three inputs, three outputs

4. How many select lines are contained in multiplexer with 1024 inputs and one output

   (a) 20 (b) 10 (c) 15 (d) 28

5. When a flip-flop is set, its output will be?

   (a) $Q=1,\overline{Q}=0$ (b) $Q=0,\overline{Q}=1$ (c) $Q=0,\overline{Q}=0$ (d) $Q=1,\overline{Q}=1$

6. The no change mode for a JK flip-flop is

(a) $J = 0, K = 1$ (b) $J = 1, K = 1$ (c) $J = 1, K = 0$ (d) $J = 0, K = 0$

7. A combinational PLD with a programmable AND array and fixed OR array is called

(a) PAL (b) ROM (c) PLA (d) None of these

8. Compute the number of 32*K* memory circuits required to construct 1*Mb* memory

(a) 16 (b) 32 (c) 8 (d) 64

9. What is HDL?

(a) Hardware description language (b) Hardware development language
(c) Hardware digital language (d) None of the above

10. Main component of a VHDL description are

(a) Entry and Package (b) Entry and Architecture
(c) Package and Architecture (d) Package and Configuration

PART - B (5 x 2 = 10 Marks)

11. State Demorgan's theorem.

12. Write truth table for half subtractor.

13. List the applications of the flip-flop.

14. Define hazards and its types.

15. List the data objects supported by VHDL.

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Explain hamming code with an example. State its advantages over parity code. (8)

(ii) Design a TTL logic circuits for a 2 input NANAD gate. (8)

Or

(b) (i) Explain weighted and non weighted codes with example. (8)

(ii) List the advantages of digital ICs. (8)

17. (a) Implement the following Boolean function using suitable

(i) Multiplexer (ii) Decoder

$F = \Sigma m\ (1, 2, 3, 5, 9, 12, 14, 15) + \Sigma d\ (4, 8, 11)$ (16)

Or

(b) Minimize the following Boolean function using K map

$F = \Sigma m\ (0, 2, 5, 7, 8, 10, 13, 15, 16, 21, 23, 24, 26, 29) + \Sigma d(1, 9, 18, 30, 31)$ (16)

18. (a) Design BCD asynchronous counter with state table and state diagrams. (16)

Or

(b) Solve and design a sequential circuit using JK flip flop for the state diagram shown in the figure 1. Use state reduction if possible. Make proper state assignment. (16)

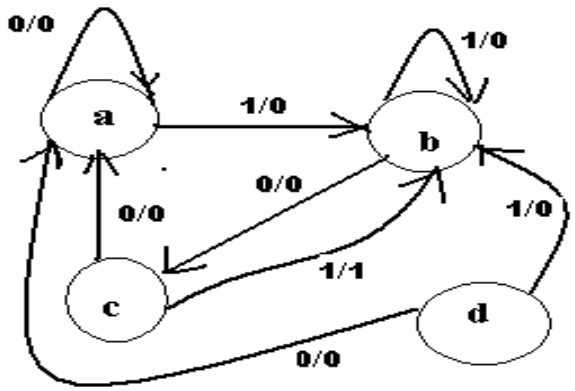

Figure1. State diagram

19. (a) Implement the following Boolean function using suitable PAL

$W(A, B, C, D) = \Sigma m(0, 2, 6, 7, 8, 9, 12, 13, 15)$

$X(A, B, C, D) = \Sigma m(0, 2, 6, 8, 9, 12, 13, 14)$

$Y(A, B, C, D) = \Sigma m(2, 3, 8, 9, 10, 12, 13)$

$Z(A, B, C, D) = \Sigma m(1, 3, 4, 6, 9, 12, 14)$ (16)

Or

(b) Develop the state diagram and state table for a logic system that has two input X and Y and one output Z, which is to behave in the following manner. Initially both input and output are equal to zero. Whenever $X = 1$ and $Y = 0$ the Z becomes 1. $X = 0$ and $Y = 1$ the Z becomes 0 $X = Y = 0$ or $X = Y = 1$ Z becomes no change. (16)

20. (a) Write a VHDL code for a Half adder circuit. (16)

Or

(b) Write a VHDL description of a D flip flop. (16)

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