**Reg. No. :** | | | | | | | | | | |

## Question Paper Code: 41342

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2016

Third Semester

Electronics and Communication Engineering

14UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The binary equivalent of decimal 41 is

   (a) 101001 (b) 101010 (c) 010111 (d) 101101

2. The simplified logic of the Boolean function $x'y'z + x'yz + xy'$ is

   (a) $x'yz+xyz$ (b) $x'z + xy'$ (c) $x'z'+ x'y'$ (d) $xz+xy$

3. The difference output of half-subtractor is

   (a) $x'y'+ xy$ (b) $xy+xy'$ (c) $xy+xy'$ (d) $x'y+xy'$

4. The circuit that generates the parity bit in the transmitter is

   (a) Parity checker (b) Parity generator

   (c) Both (a) and (b) (d) None of these

5. The characteristic equation of D-flip-flop

   (a) $Q(t + 1) = D + 1$ (b) $Q(t + 1) = D$
   (c) $Q(t + 1) = D'$ (d) $Q(t + 1) = D'Q$

6. How many flip-flops are required to design mod-6 counter?

   (a) 4 (b) 6 (c) 3 (d) 8

7. The limit of a noise voltage which may be allowed in the circuit is

(a) Noise Margin (b) Noise Voltage
(c) Low level input noise (d) High level input noise

8. The PLD with programmable AND array and fixed OR array is

(a) PAL (b) PLA (c) PROM (d) CPLD

9. The number of state variable '*m*' produces

(a) $2^{m+1}$ states (b) $2^{m-1}$ states (c) $2^{m}$ states (d) None

10. In this mode the inputs and outputs are represented by levels

(a) Fundamental mode (b) Pulse mode
(c) Both (a) and (b) (d) None of these

PART - B (5 x 2 = 10 Marks)

11. Obtain the canonical sum of product form of the function: $Y=AB + ACD$.

12. With truth table draw the circuit of 3-bit odd parity generator.

13. Write the excitation table of RS flip-flop.

14. Describe RAM and give its types.

15. Give the general model of ASM.

PART - C (5 x 16 = 80 Marks)

16. (a) Simplify the following Boolean function by Quine-McCluskey method:

$F = \Sigma (0, 1, 2, 8, 10, 11, 14, 15)$. (16)

Or

(b) (i) Simplify the Boolean function using K-map

$F (w, x, y, z) = \Sigma (0, 1, 2, 4, 5, 6, 8, 9, 12, 13, 14)$. (8)

(ii) Implement the following function with NAND gate only

$F (x, y, z) = \Sigma (0, 6)$. (8)

17. (a) (i) With logic diagram Truth table and explain about 3-to-8 decoder. (6)

(ii) Define multiplexer and implement the Boolean function with a suitable multiplexer.

$F (A, B, C, D) = \Sigma (0, 1, 3, 4, 8, 9, 15)$. (10)

Or

(b) With Truth table, design BCD-to-excess-3 code converter and obtain its logic diagram. (16)

18. (a) (i) With neat diagram explain in detail about how the race around condition is avoided in master-slave JK flip-flop. (8)

(ii) Design 4-bit asynchronous up-down binary counter using T flip-flop. (8)

Or

(b) (i) Realize D flip-flop using SR flip-flop. (8)

(ii) With neat illustration explain in detail about 4-bit parallel-in-serial out shift register. (8)

19. (a) With block diagram explain about PLA and realize the following functions in PLA:

$$F1 = \overline{A}\ B\ \overline{C} + A\ \overline{B}\ C + \overline{A}\ B\ C$$
$$F2 = A\ B + AC + \overline{A}BC$$

(16)

Or

(b) (i) Differentiate registered PAL and configurable PAL (8)

(ii) Design a 4-bit binary–to gray code converter using PROM. (8)

20. (a) Design serial binary adder using D-flip-flop. (16)

Or

(b) Design an asynchronous sequential circuit with two inputs $x_1$ and $x_2$ and one output $Z$. Initially, both inputs are equal to zero. When $x_1$ or $x_2$ becomes '1' the output $Z$ becomes 1.When the second input also becomes 1, the output changes to 0. The output stays at 0 until the circuit goes back to the initial state. (16)

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