Reg. No. : | | | | | | | | | | |

Question Paper Code: 31342

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2016

Third Semester

Electronics and Communication Engineering

01UEC302 - DIGITAL ELECTRONICS AND DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Use Boolean algebra to simplify the function $f = x(y + wz) + wxz$. Sketch the logic circuit for the minimized function using NAND gates.
2. Represent the following numbers in binary: (i) $(673.124)_8$ and (ii) $(306.D)_{16}$.
3. Write the truth table for half-adder and full-adder.
4. List any four applications of multiplexer.
5. Differentiate the combinational logic from sequential logic.
6. Write the characteristic equation of SR flip-flop and T flip-flop.
7. Mention the advantages of dynamic RAM over static RAM.
8. Design the logic diagram of a 2 input NAND gate using CMOS logic.
9. What is an excitation table?
10. Distinguish between Mealy and Moore state machines.

PART - B (5 x 16 = 80 Marks)

11. (a) Simplify the following expression $F(w, x, y, z) = \sum_m (1, 3, 4, 5, 9, 10, 11) + \sum_d (6, 8)$ using Quine – McCluskey method. (16)

Or

(b) Simplify the logic function $F(A, B, C, D) = \sum_m(0, 1, 2, 5, 6, 8) + d(3, 4, 7, 14)$ using K-map in SOP and POS form. Sketch the logic circuit for SOP and POS form. Infer which form is cost-effective. (16)

12. (a) (i) Design and implement a full subtractor using 3 x 8 decoder. (6)

(ii) Implement the logic expression $F = \Sigma m$ (0, 2, 4, 7) using 4x1 MUX and 8x1 MUX. (10)

Or

(b) (i) Explain the design and working of binary adder and carry look-ahead adder circuit. (8)

(ii) Design and implement a 4 bit magnitude comparator using logic gates. (8)

13. (a) Explain the operation of D and T-flip flops. Write the truth table and draw their waveforms. Design the D and T-flip flops using JK flip flop. (16)

Or

(b) (i) Design a modulo-6 counter with asynchronous reset using T flip flop. Illustrate its operation using timing diagram. (8)

(ii) Draw the logic circuit diagram of universal shift register and explain its functional operation with functional table. (8)

14. (a) Implement the following Boolean functions using ROM, PLA and PAL $F1(A, B, C) = \Sigma m$ (0, 1, 3, 5) and $F2 (A, B, C) = \Sigma m$ (0, 3, 5, 7). (16)

Or

(b) (i) Explain the architecture and design procedure of Programmable Logic Array (PLA) and Programmable Array Logic (PAL) with neat logic circuit diagram. (12)

(ii) Compare the PROM, PLA and PAL. (4)

15. (a) (i) Explain the hazards in sequential circuits with appropriate examples. (8)

(ii) Design a 5 state sequential machine whose sequential states are: 000, 001, 010, 110, 111, 000 … Assume initial state is 000. (8)

Or

(b) Design a clocked sequential circuit with single input X and single output Z. The circuit produces an output Z=1 whenever the input X completes the sequence 10111 and overlapping is allowed. Obtain the state transition table and implement using D flip-flops. (16)