Reg. No. :

Question Paper Code: 41437

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2016

Fourth Semester

Computer Science and Engineering

14UEC423 - MICROPROCESSORS AND MICROCONTROLLERS

(Common to Information Technology)

(Regulation 2014)

Duration: Three hours

Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

- 1. SUB B instruction in 8085 microprocessor
 - (a) resets the carry and sign flag
 - (b) sets the zero and parity flag
 - (c) sets the zero and carry flag
 - (d) can modify all flags according to result
- 2. When a CALL instruction is executed, the stack pointer register is
 - (a) decremented by two (b) incremented by two
 - (c) decremented by one (d) incremented by one

3. The 8086 has a

- (a) 16-bit data bus and 20-bit address bus
- (b) 8-bit data bus and 20-bit address bus
- (c) 16-bit data bus and 16-bit address bus
- (d) 8-bit data bus and 16-bit address bus
- 4. Which of the following instruction is a logical instruction?

(a) DIV AB (b) TEST (c) CALL (d) AAM

| 5. | The 8087 coprocessor oper instruction | rate in | with an 8086 processor and with the same | | | | | |
|---|--|--|--|--------------------|--|--|--|--|
| | (a) series, byte (b) parallel, byte | | yte | | | | | |
| | (c) series, bits | | (d) parallel, bi | (d) parallel, bits | | | | |
| 6. | The synchronization between processor and coprocessor can be done by | | | | | | | |
| | (a) RQ/GT_0 and RQ/GT_1 , FWAIT | | (b) INT and NMI, WAIT | | | | | |
| | (c) BUSY and TEST, FWAIT | | (d) S_0 and QS_0 , WAIT | | | | | |
| 7. | How many address lines are required to access 1 MB RAM using microprocessor? | | | | | | | |
| | (a) 16 | (b) 8 | (c) 20 | (d) 12 | | | | |
| 8. | The 8279 is a | | | | | | | |
| | (a) DMA controller(c) counter | (b) programmable keyboard display interface(d) interrupt controller | | | | | | |
| 9. | Which of the following registers can be used as two individual 8-bit registers? | | | | | | | |
| | (a) DPTR | (b) PC | (c) SBUF | (d) PSW | | | | |
| 10. |). What will be the output after execution of the following instruction? MOV A, #55 ANL A, #67 | | | | | | | |
| | (a) 54 | (b) 45 | (c) 55 | (d) 67 | | | | |
| PART - B (5 x 2 = 10 Marks) | | | | | | | | |
| 11. | 11. Classify the signals of 8085. | | | | | | | |
| 12. | 12. List out the flags present in 8086. | | | | | | | |
| 13. Compare closely coupled and loosely coupled configurations of co-processor. | | | | | | | | |
| 14. | 14. Highlight the method used to transfer large blocks of data between external device and memory at high speed. | | | | | | | |
| 15. | 5. Draw the format of PSW of 8051. | | | | | | | |
| PART - C (5 x 16 = 80 Marks) | | | | | | | | |
| 16. | 5. (a) Draw and explain the architecture of 8085 microprocessor. (16 | | | | | | | |

Or

| | (b) | (i) Write an ALP to convert binary to decimal number using 8085. | (10) | | | | |
|-----|-----|--|-------|--|--|--|--|
| | | (ii) Write various instruction set of 8085. | (6) | | | | |
| 17. | (a) | (i) Explain the various addressing modes of 8086. | (12) | | | | |
| | | (ii) Describe assembler directives. | (4) | | | | |
| Or | | | | | | | |
| | (b) | Explain in detail about Interrupt Service Routine (ISR) of 8086 processor. | (16) | | | | |
| 18. | (a) | Draw the architecture of 8087 numeric data processor and explain each block. | (16) | | | | |
| | Or | | | | | | |
| | (b) | Explain the architecture of 8089 I/O processor with a diagram. | (16) | | | | |
| 19. | (a) | Apply 8085 microprocessor for interfacing stepper motor control system and | write | | | | |
| | | an assembly language program for speed control. | (16) | | | | |
| Or | | | | | | | |
| | (b) | Describe the block diagram of IC 8237 DMA controller. | (16) | | | | |
| 20. | (a) | Draw the architecture of 8051 microcontroller and explain each block. | (16) | | | | |
| Or | | | | | | | |
| | (b) | Explain the interfacing of ADC and DAC with 8051 microcontroller. | (16) | | | | |

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