Reg. No. : | | | | | | | | | | |

Question Paper Code: 31941

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2016

Elective

Electronics and Communication Engineering

01UEC903 - COMPUTER ARCHITECTURE AND ORGANIZATION

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Discuss the stored program concept.
2. List out the register level circuit components.
3. Point out the advantages of Co-processors.
4. Compare spatial expansion and temporal expansion.
5. What is microprogramming?
6. What is Write-After-Write (WAW) hazard?
7. Write about associative memory.
8. Define Hit ratio.
9. List out the limitations of the programmed I/O data transfer method.
10. How many 128 * 4 RAM memory chips are required to construct RAM memory system of 1 *Kbytes*?

PART - B (5 x 16 = 80 Marks)

11. (a) Briefly explain the organization of CPU and memory of the IAS computer with instruction set. (16)

Or

(b) (i) Write in detail about various addressing modes. (8)

(ii) Explain zero, one, two and three addressing instructions with example. (8)

12. (a) State the advantages of sequential ALU over combinational ALU for multiplier and divider operation. Also discuss the structure of basic sequential ALU. (16)

Or

(b) (i) With a neat block diagram explain in detail about CPU-coprocessor interfacing. (10)

(ii) Write short notes on pipeline processing. (6)

13. (a) Explain the design of micro-programmed control unit for the two's complement multiplier with a diagram. (16)

Or

(b) Explain with a diagram the organization of a CPU incorporating a four stage instruction pipeline. (16)

14. (a) (i) Design the following RAM using N x w bit IC RAM.

(1) N x 4w bit RAM

(2) 4N x w bit RAM (10)

(ii) Write short notes on optical memories. (6)

Or

(b) Explain the concepts of memory hierarchies. (16)

15. (a) List out the three bus arbitration schemes. Explain any two with a diagram. (16)

Or

(b) (i) With a diagram explain static and dynamic redundancy for designing fault tolerant system. (10)

(ii) Compare RISC and CISC processor. (6)