Reg. No. : | | | | | | | | | | |

Question Paper Code: 41356

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2016

Third Semester

Electronics and Instrumentation Engineering

14UEI306 - DIGITAL ELECTRONICS

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. How is a *J-K* flip-flop made to toggle?

   (a) $J = 0, K = 0$ (b) $J = 1, K = 0$ (c) $J = 0, K = 1$ (d) $J = 1, K = 1$

2. Which of the following is correct for a gated D flip-flop?

   (a) The output toggles if one of the inputs is held high
   (b) Only one of the inputs can be high at a time
   (c) The output complement follows the input when enabled
   (d) *Q* output follows the input *D* when the enable is high

3. When is a flip-flop said to be transparent?

   (a) when the *Q* output is opposite the input
   (b) when the *Q* output follows the input
   (c) when you can see through the IC packaging
   (d) None of these

4. The systematic reduction of logic circuits is accomplished by

   (a) using Boolean algebra (b) symbolic reduction
   (c) TTL logic (d) using a truth table

5. What is the meaning of RAM, and what is its primary role?

   (a) Readily Available Memory; it is the first level of memory used by the computer in all of its operations
   (b) Random Access Memory; it is memory that can be reached by any sub- system within a computer, and at any time
   (c) Random Access Memory; it is the memory used for short-term temporary data storage within the computer
   (d) Resettable Automatic Memory; it is memory that can be used and then automatically reset, or cleared, after being read from or written to

6. What is a major disadvantage of RAM?

   (a) Its access speed is too slow
   (b) Its matrix size is too big
   (c) It is volatile
   (d) High power consumption

7. In positive logic, _____

   (a) a HIGH = 1, a LOW = 0
   (b) a LOW = 1, a HIGH = 0
   (c) only HIGHs are present
   (d) only LOWs are present

8. For JK flip flop with J=1, K=0, the output after clock pulse will be _____

   (a) 0 (b) 1 (c) High Impedance (d) No change

9. For which of the following two inputs, The NOR gate output will be low

   (a) 01 (b) 10 (c) 11 (d) all the above

10. How many select lines will a 16 to 1 multiplexer will have

    (a) 4 (b) 32 (c) 5 (d) 1

PART - B (5 x 2 = 10 Marks)

11. Simplify: $A + AB + \overline{A} + B$.

12. Write the truth table of a 4:1 multiplexer.

13. Define synchronous counter.

14. Define primitive flow table.

15. Draw the basic dynamic memory cell.

PART - C (5 x 16 = 80 Marks)

16. (a) Simplify the Boolean function using tabulation method.
Y (A, B, C, D)= ∑ m (1, 2, 3, 5, 9, 12, 14, 15)+∑ D (4, 8, 11). (16)

Or

(b) (i) Minimize the four variable logic function using K-map
F(A, B, C, D)= ∑ m (0, 1, 2, 3, 5, 7, 8, 9, 11, 14). (8)

(ii) Convert the decimal number 41 into its equivalent binary, hexadecimal, octal and gray code. (4)

(iii) Using Boolean laws and rules, simplify the logic expression.
$Z = (\overline{A} + B)(A + B)$. (4)

17. (a) (i) Implement $F = (A\overline{B} + \overline{A}B)(C + \overline{D})$ using only NOR gates. (10)

(ii) Implement a Half adder. (6)

Or

(b) (i) Design a 2-bit magnitude comparator which A_1, A_0 and B_1, B_0. (10)

(ii) Implement full subtractor using demultiplexer. (6)

18. (a) (i) How will you convert a D flip flop into JK flip flop? (8)

(ii) Sketch a 4-bit serial in serial out shift register and draw its waveforms. (8)

Or

(b) Design a synchronous decade counter using T flip flop. (16)

19. (a) Design an asynchronous sequential circuit with two inputs *X* and *Y* and with one output *Z*. Whenever *Y* is 1, input *X* is transferred to *Z*. When *Y* is 0, the output does not change for any change in *X*. (16)

Or

(b) What is a hazard? Explain the different types of hazards. Discuss in detail how hazards can be eliminated. (16)

20. (a) Explain about RAM and its types. (16)

Or

(b) Explain about programmable logic array. Implement the following Boolean function with a PLA

$F_1 (A, B, C) = \sum (0, 1, 2, 4)$

$F_2 (A, B, C) = \sum (0, 5, 6, 7)$

$F_3 (A, B, C) = \sum (0, 3, 5, 7)$ (16)