Reg. No. : | | | | | | | | | | |

Question Paper Code: 41323

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2016

Third Semester

Computer Science and Engineering

14UCS303 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The BSA instruction is

   (a) Branch and Store Accumulator (b) Branch and Save return Address
   (c) Branch and Shift Address (d) Branch and Show Accumulator

2. Content of the program counter is added to the address part of the instruction in order to obtain the effective address is called

   (a) relative address mode (b) index addressing mode
   (c) register mode (d) implied mode

3. The 2's compliment form (Use 6 bit word) of the number 1010 is

   (a) 111100 (b) 110110 (c) 110111 (d) 1011

4. Floating point representation is used to store

   (a) Boolean values (b) whole numbers
   (c) real integers (d) integers

5. An instruction pipeline can be implemented by means of

   (a) LIFO buffer (b) FIFO buffer (c) Stack (d) None of these

6. The registers, the ALU, and the interconnecting bus are collectively referredto as the _____

(a) Datapath (b) Subpath
(c) Connecting path (d) None of these

7. Multithreading an interactive program will increase responsiveness to the user by

(a) continuing to run even if a part of it is blocked
(b) waiting for one part to finish before the other begins
(c) asking the user to decide the order of multithreading
(d) None of these

8. The cost of parallel processing is primarily determined by

(a) time complexity (b) switching complexity
(c) circuit complexity (d) none of the above

9. The idea of cache memory is based

(a) on the property of locality of reference
(b) on the heuristic 90-10 rule
(c) on the fact that references generally tend to cluster
(d) all the above

10. Virtual memory consists of

(a) Static RAM (b) Dynamic RAM
(c) Magnetic memory (d) None of these

PART - B (5 x 2 = 10 Marks)

11. Distinguish between auto increment and auto decrement addressing mode.

12. What is the IEEE standard for binary floating point numbers?

13. How do you handle the data hazard?

14. What are the Flynn's classifications?

15. What do you mean by memory mapped input/output?

PART - C (5 x 16 = 80 Marks)

16. (a) What do you mean by addressing modes? Explain the types of addressing modes that exists in modern processors? (16)

Or

(b) (i) Discuss the factors influencing in performance. (8)

(ii) Explain in detail the different instruction formats with examples. (8)

17. (a) (i) Explain the rules for basic arithmetic operations of floating point numbers? (8)

(ii) Explain Guard bit and Truncation? (8)

Or

(b) (i) Illustrate non-restoring division algorithm with an example. (8)

(ii) Design a 16-bit carry- look ahead adder using 4-bit adders and explain. (8)

18. (a) What are the hazards of conditional branches in pipelines? How it can be resolved? (16)

Or

(b) Explain the super scalar operations with a neat diagram. (16)

19. (a) What is instruction-level parallelism? Explain in detail about the various dependences caused by instruction - level parallelism? (16)

Or

(b) Explain in details multi- core processor with one example. (16)

20. (a) (i) What is bus arbitration? Describe the centralized approach for bus arbitration with help of diagram. (8)

(ii) Explain the need for memory hierarchy technology, with a four-level of memory. (8)

Or

(b) Explain the virtual memory address translation with necessary tables and diagrams. (16)
