Reg. No. : | | | | | | | | | | |

Question Paper Code: 31323

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2016

Third Semester

Computer Science and Engineering

01UCS303 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Differentiate Big endian and Little endian format.
2. For the following *C* statement, what is the corresponding MIPS assembly code? Assume that the variables *f*, *g* and *h* are given and could be considered 32-bit integers as declared in a C program. Use a minimal number of MIPS assembly instructions $f = g + (h - 5)$.
3. Draw the IEEE single and double precision floating point formats.
4. Define Exception.
5. What is mean by hazard?
6. List out the advantages of pipelining.
7. Write short note about speculative execution.
8. Define hardware multithreading.
9. Distinguish cache memory and virtual memory.
10. What is mean by interrupt?

PART - B (5 x 16 = 80 Marks)

11. (a) Explain the logical and control operations in MIPS assembly language in detail. (16)

Or

(b) (i) What is mean by addressing modes? Explain the MIPS addressing modes in detail with neat diagram and example. (8)

(ii) What are the ideas should be considered in terms of computer design? Describe in detail. (8)

12. (a) (i) Explain the sequential version of the multiplication algorithm and hardware. (10)

(ii) Perform the 0100 * 0011 using sequential multiplier and show all the steps. (6)

Or

(b) Explain the floating point addition steps and algorithm in detail. (16)

13. (a) What are the control signals used in the MIPS processor? Explain the datapath in operation for a load instruction. (16)

Or

(b) (i) Explain the basic concepts of pipelining and compare it with sequential processing. Draw wherever necessary diagrams. (6)

(ii) Discuss in detail how branch hazard can be resolved. (10)

14. (a) Explain the techniques to exploit Instruction Level Parallelism (ILP) in detail. (16)

Or

(b) (i) Explain the Flynn's classification in detail. (10)

(ii) Write short notes on multicore processor. (6)

15. (a) Explain the following:

(i) Cache write strategy (4)

(ii) Cache write replacement strategies (4)

(iii) Cache block replacement (8)

Or

(b) Explain the concept of DMA in detail with a neat sketch. (16)

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