Reg. No. : | | | | | | | | | | |

Question Paper Code: 21008

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2014.

Second Semester

Computer Science and Engineering

01UCS207- DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Which gates are called as the universal gates? What are their advantages?
2. Convert $(25.35)_{10}$ into its octal equivalent.
3. State the importance of tabulation method?
4. What do you mean by comparator?
5. Define HDL.
6. What is programmable logic array? How does it differ from ROM?
7. Give the classification of PLDs.
8. Give the comparison between synchronous and asynchronous counters.
9. What is the operation of T flip-flop? Illustrate using truth table.
10. Define state table.

PART - B (5 x 16 = 80 Marks)

11. (a) (i) List out the advantages and disadvantages of K-map method. (8)

(ii) Name the basic laws and axioms in boolean algebra with necessary equations. (8)

Or

(b) Design Half adder and full adder circuits with truth table, logic diagram and their operation. (16)

12. (a) Design a logic circuit that accepts a 4-bit gray code and converts it into 4-bit binary code with suitable example. (16)

Or

(b) Explain the different type of binary codes with suitable examples. (16)

13. (a) (i) Construct a 16x1 multiplexer with two 8x1 and one 2x1 multiplexers. Use appropriate diagrams. (10)

(ii) With neat diagram, explain the types of memory. (6)

Or

(b) With neat diagrams, explain multiplexer and demultiplexer circuits. (16)

14. (a) (i) Write the procedure for analyzing a clocked sequential circuit with JK flip flop. (8)

(ii) Design a sequential mod-7 counter. (8)

Or

(b) (i) Explain in detail about parallel in serial out shift register, with neat sketches. (10)

(ii) Write the HDL for full adder circuits. (6)

15. (a) (i) Describe the design procedure for asynchronous sequential circuits. (10)

(ii) Write short notes on ASM chart. (6)

Or

(b) Explain the method for the minimization of primitive flow table with an example. (16)