Reg. No. : | | | | | | | | | | |

Question Paper Code: 92071

M.E. DEGREE EXAMINATION, DECEMBER 2013.

Elective

VLSI Design

01PVL507 - ASIC DESIGN TECHNIQUES

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Write the design flow of ASIC.
2. What is transistor parasitic capacitance?
3. Write short notes on static RAM.
4. Give the PREP bench mark for programmable ASIC.
5. Draw the structure of FPGA design flow.
6. What is meant by CFI design representation?
7. Write the types of fault simulation.
8. What is meant by logic strength?
9. What are the steps involved in min-cut algorithms?
10. Write the goal and objectives of detailed routing.

PART - B (5 x 14 = 70 Marks)

11. (a) Explain the different types of ASIC with neat diagram. (14)

Or

(b) Describe the datapath logic cell structure with suitable example. (14)

12. (a) Discuss the concept and types of antifuse. (14)

Or

(b) Draw and explain the configurable logic block of any two xilinx LCA series. (14)

13. (a) Write short notes on.

i) FPGA synthesis (7)

ii) Schematic entry. (7)

Or

(b) Explain the electronic design interchange format in detail. (14)

14. (a) Explain the boundary scan testing in detail. (14)

Or

(b) Discuss the concept of automatic test pattern generation with an example. (14)

15. a) Describe about the FPGA partition in detail. (14)

Or

(b) Explain the concepts and partition steps in floor planning. (14)

PART - C (1 x 10 = 10 Marks)

16. (a) Test a comparator circuit using boundary scan method. (10)

Or

(b) Explain the design flow for the xilinx implementation of the halfgate ASIC . (10)