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Question Paper Code: 12074

M.E. DEGREE EXAMINATION, DECEMBER 2013.

First Semester

VLSI Design

01PVL103 VLSI DESIGN TECHNIQUES

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Draw the cross-sectional view of twin-tub inverter structure.
2. Define threshold voltage of a MOS transistor.
3. Write any two rules followed in drawing stick diagrams.
4. Give the general expression of transconductance (g_m) for MOS transistors.
5. Determine the worst case capacitance at the input assuming a step input signal for a 3 input NAND logic circuit. Consider an inverter with $\beta_n = \beta_p$, used as a sizing reference.
6. State the factors which affect the rise time and fall time in a CMOS inverter.
7. Construct a 2-input multiplexer using CMOS logic gates.
8. A 8 bit ripple carry adder suffers a huge delay in producing a carry. Suggest a suitable logic circuit to speedup the addition process.
9. Distinguish between continuous assignment and procedural assignment in statements.
10. Write a Verilog code for a 4 x 2 encoder.

PART - B (5 x 14 = 70 Marks)

11. (a) Explain the fabrication process of n-well process with neat sketch. (14)

Or

(b) Derive I_{ds} versus V_{ds} relationship for an NMOS transistor and explain the sub threshold region, triode region and saturation region. (14)

12. (a) In the inverter circuit, what is meant by $Z_{p.u}$ and $Z_{p.d}$? Derive the required ratio between $Z_{p.u}$ and $Z_{p.d}$ if an nMOS inverter is to be driven by another nMOS inverter. (14)

Or

(b) (i) Draw the DC characteristics of the CMOS inverter showing all the critical points and derive an equation for its mid-point voltage. (7)

(ii) Implement the function $Y = \overline{(\bar{A}B + AD)C + D}$ in CMOS logic using minimum number of transistors. Examine its transient behavior by comparing with a reference symmetrical CMOS inverter and perform sizing if needed. (7)

13. (a) (i) A new CMOS system is advertised as having a complexity of 250,000 transistors, uses a 34MHz clock, and operates from a 3V supply. Assume the system is composed entirely of gates with an average of five transistors per gate and that the average gate capacitance is 0.1 pF. Calculate the dynamic power dissipated by this chip.) (5)

(ii) A chip operating with 5V at 120MHz with an internal switched capacitance of 400pF, assume the average rise time/fall time is 250ps. Calculate the dynamic and short-circuit power dissipated in the chip. How does the short –circuit dissipation change if the average rise/fall time is 550ps? (9)

Or

(b) What is precharge mode and evaluation mode? Explain the working of Dynamic CMOS logic with an example. (14)

14. (a) Consider an 8X1 Multiplexer that is constructed using Multiplexers as primitives.

i) Construct an 8X1 multiplexer using 2X1 multiplexers.

ii) Select a logic circuit to implement the design.

iii) Apply the Logical Effort to designing the gates if the output of the 8X1 multiplexer is to drive a capacitor C_{out} that is $12C_{inv}$, where C_{inv} is the capacitance of a unit inverter. Assume that the gates are built using static CMOS circuits. (14)

Or

(b) (i) Design a 4-bit Braun array multiplier using full adders and AND gates. (7)

(ii) Design a 4-bit Carry Look-Ahead adder and explain with relevant expressions. (7)

15. a) Design a 3X8 active low decoder using NAND gates. Write a Verilog description using structural modeling and modify your code to include an enable input. (14)

Or

(b) Construct a 4-bit Baugh wooley multiplier and write Verilog test bench for the same. (14)

PART - C (1 x 10 = 10 Marks)

16. (a) Design a CMOS inverter with Supply Voltage of 1.2V, $V_{tn} = |V_{tp}| = 0.5V$

i) V_M=0.7V

ii) V_M=0.5V

iii) What happens to the propagation delays t_{PHL} and t_{PLH} in these two cases? (10)

Or

(b) Write the sizing of each transistor for the functions X and Y to achieve symmetric design with respect to symmetric inverter. Assume $\mu_n = 2.4\mu_p$.

i) $X = \overline{AC + BC + DE}$

ii) $Y = \overline{(P+Q)(M+N)(T+U)}$ (10)