Reg. No. : | | | | | | | | | | |

Question Paper Code: 12032

M.E. DEGREE EXAMINATION, DECEMBER 2013.

First Semester

Computer Science and Engineering

01PCS101-COMPUTER ORGANIZATION AND DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 2 = 20 Marks)

1. Define Instruction Set Architecture (ISA).
2. Give the conditions to overcome the data hazard.
3. Define loop level parallelism.
4. What is branch prediction?
5. What is meant by control dependence?
6. What are the limitations of ILP?
7. Define Multithreading.
8. What is meant by Symmetric Shared Memory?
9. What is meant by Read miss?
10. Define temporal locality.

PART - B (5 x 14 = 70 Marks)

11. (a) Explain about the quantitative principles involved in computer design. (14)

Or

(b) Explain the basic operations of a four stage pipelining with a neat diagram. (14)

12. (a) Explain the methods to overcome data hazards with dynamic scheduling. (14)

Or

(b) Explain in detail about hardware based speculation in ILP. (14)

13. (a) Explain about static branch prediction with suitable illustrations. (14)

Or

(b) Explain about VLIW with suitable illustrations. (14)

14. (a) Explain about Symmetric Shared Memory Architecture with example. (14)

Or

(b) Explain about synchronization in multiprocessor with suitable example. (14)

15. (a) Explain the suitable method to reduce cache miss penalty and miss rate. (14)

Or

(b) Explain about various I/O performance measures. (14)

PART - C (1 x 10 = 10 Marks)

16. (a) Explain RAID architecture with suitable illustrations. (10)

Or

(b) Explain the implementation of SMT and CMP architecture. (10)

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