Reg. No. : | | | | | | | | | | |

Question Paper Code: 41632

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Third Semester

Instrumentation and Control Engineering

14UIC302 – DIGITAL LOGIC CIRCUITS AND DESIGN

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions.

PART A - (10 x 1 = 10 Marks)

1. The Hexadecimal equivalent of a decimal number 48 is

   (a) 2B (b) 2E (c) 2F (d) F2

2. How many outputs are on a BCD decoder?

   (a) 4 (b) 16 (c) 8 (d) 10

3. What is ROM?

   (a) repeat on memory (b) read on memory
   (c) read only memory (d) repeat only memory

4. In PROM, we can

   (a) store the data once and read multiple times (b) store and erase data once
   (c) store and erase data multiple times (d) store once and read once

5. Which type of gate can be used to add two bits?

   (a) Ex-OR (b) Ex-NOR (c) Ex-NAND (d) NOR

6. How many flipflops are required to build a binary counter that counts from 0 to 1023?

   (a) 12 (b) 20 (c) 50 (d) 10

7. The next state variables in asynchronous sequential circuits are called

(a) secondary variables (b) excitation variables
(c) primary variables (d) short term memory

8. In ASM, the decision box is represented by

(a) circle (b) oval (c) diamond (d) rectangle

9. Which of the following logic family has the shortest propagation delay?

(a) CMOS (b) NMOS (c) ECL (d) 74Sxx

10. The VHDL is based on the _____ library

(a) IEE (b) WORK (c) IEEE (d) Standard

PART - B (5 x 2 = 10 Marks)

11. State Demorgan's Theorem.

12. Define fan in and fan out.

13. Compare combinational and sequential circuits

14. What is race around condition?

15. List the advantages of CMOS logic.

PART - C (5 x 16 = 80 Marks)

16. (a) Reduce the Boolean function using k-map technique and implement using gates $f(w, x, y, z) = \sum m(0, 1, 4, 8, 9, 10)$ which has the don't cares condition $d(w, x, y, z) = \sum m(2,11)$. (16)

Or

(b) Use Quine–Mc cluskey method and simply the following function, $f(a, b, c, d) = \sum m(0, 1, 2, 3, 8, 9)$. (16)

17. (a) Design and draw 4 bit binary to gray code converter and explain. (16)

Or

(b) Explain in detail about PLA with a specific example. (16)

18. (a) Design a four state down counter using T flip flop. (16)

Or

(b) Construct a decade ripple counter using flip flops and explain. (16)

19. (a) Draw the fundamental mode asynchronous circuit and explain in detail. (16)

Or

(b) Explain with neat diagram the different hazards and the way to eliminate them. (16)

20. (a) Explain the various modeling methods used in VHDL with an example. (16)

Or

(b) What is VHDL? Design a full adder circuit using VHDL code. (16)

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