Reg. No. : | | | | | | | | | | |

Question Paper Code: 50336

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Third Semester

Electrical and Electronics Engineering

15UEE306 - DIGITAL LOGIC CIRCUITS

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The universal gate is

   (a) OR gate (b) NAND gate
   (c) AND gate (d) NOT gate

2. Which is not part of emitter-coupled logic (ECL)?

   (a) Differential amplifier (b) Bias circuit
   (c) Emitter-follower circuit (d) Totem pole circuit

3. Which of the following expressions is in the form of product of sums form

   (a) (A+B)(C+D) (b) (AB)+(CD)
   (c) AB(CD) (d) AB+CD

4. A decoder can be used as demultiplexer by

   (a) Tying all enable pins LOW
   (b) Tying all data-select lines LOW
   (c) Tying all data-select lines HIGH
   (d) Using the input lines for data selection and enable line for data input

5. In Moore model outputs are functions of

   (a) Present state (b) Input state
   (c) Next state (d) Both a and b

6. Memory elements in clocked sequential circuits are called as

(a) Latches (b) Flip-flop
(c) Signals (d) Totem pole circuit

7. Once a PAL have been programmed

(a) It cannot be reprogrammed (b) Its outputs are only active HIGHs
(c) Its outputs are only active LOWs (d) Its logic capacity is lost

8. Race in which stable state depends on order is called

(a) Critical race (b) Identical race
(c) Non critical race (d) Defined race

9. In VHDL, the macro functions are

(a) Digital circuits (b) Analog circuits
(c) A set of bit variables (d) Preprogrammed TTL devices

10. In VHDL, which object is used to connect entities together for the model formation

(a) Constant (b) Variable (c) Signal (d) All of the above

PART - B (5 x 2 = 10 Marks)

11. State Demorgan's theorem.

12. Mention any two applications of Multiplexer.

13. Name the different types of triggering employed in a flip-flop.

14. What is programmable logic array?

15. What are the VHDL structural elements?

PART - C (5 x 16 = 80 Marks)

16. (a) Explain the operation parity generation and checking. (16)

Or

(b) Explain the operation of TTL with neat circuit diagram for 2 input NAND gate with Tottem pole output. (16)

17. (a) Simplify the Boolean function $F(w,x,y,z) = \sum m(0,1,2,4,5,6,8,9,12,13,14)$. (16)

Or

(b) Design three to eight line decoder using logic gates. (16)

18. (a) Using D-flip flop, design a synchronous counter which counts in the sequence 000, 001, 010, 011, 100, 101, 110, 111, 000. (16)

Or

(b) Explain the working of JK flip-flop with its characteristics equation, characteristics table and logic diagram. (16)

19. (a) Discuss the different types of hazards that occurs in asynchronous sequential circuits and combinational circuits. (16)

Or

(b) Implement the Boolean functions with a PAL $F_1(A,B,C) = \sum m(0,1,2,4)$. (16)

20. (a) Explain the design of Register Transfer Level (RTL) in VHDL. (16)

Or

(b) Write the VHDL coding for mod 6 counter. (16)

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