Reg. No. : | | | | | | | | | | |

Question Paper Code: 41336

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Third Semester

Electrical and Electronics Engineering

14UEE306 - DIGITAL LOGIC CIRCUITS

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. Convert hexadecimal value 16 to decimal.

   (a) 22 (b) 16 (c) 10 (d) 20

2. The difference of 111 – 001 equals.

   (a) 100 (b) 111 (c) 001 (d) 110

3. How is a JK flip-flop made to toggle?

   (a) J=0, K=0 (b) J=1, K=0 (c) J=0, K=1 (d) J=1, K=1

4. How many flip-flops are required to produce a divide-by-128 device?

   (a) 1 (b) 4 (c) 6 (d) 7

5. The terminal count of a typical modulus-10 binary counter is

   (a) 0000 (b) 1010 (c) 1001 (d) 1111

6. How many flip-flops are required to make a MOD-32 binary counter?

   (a) 3 (b) 4 (c) 5 (d) 6

7. Which type of PLD should be used to program basic logic functions?

   (a) PLA (b) PAL (c) CPLD (d) SLD

8. PROM is a

(a) non-volatile memory (b) secondary memory
(c) volatile memory (d) small memory

9. A combinational circuit that selects one from many inputs

(a) encoder (b) decoder
(c) multiplexer (d) demultiplexer

10. One application of a digital multiplexer is to facilitate

(a) data generation (b) serial-to-parallel conversion
(c) parity checking (d) data selector

PART - B (5 x 2 = 10 Marks)

11. Determine $(377)_{10}$ in Octal and Hexa-Decimal equivalent.

12. Design a half subtractor.

13. Differentiate between Mealy and Moore models.

14. What is PROM?

15. Write VHDL behavioral model for D flip-flop.

PART - C (5 x 16 = 80 Marks)

16. (a) Given that a frame with bit sequence 1101011011 is transmitted, it has been received as 1101011010. Determine the method of detecting the error using any one error detecting code. (16)

Or

(b) With circuit schematic explain the operation of a two input TTL NAND gate. (16)

17. (a) Design a full adder using two half-adders and an OR gate. (16)

Or

(b) Design a BCD to Excess 3 code converter. (16)

18. (a) Explain the circuit of a SR flip-flop and explain its operation. (16)

Or

(b) Design a serial adder using Mealy state model. (16)

19. (a) Describe the steps involved in design of asynchronous sequential circuit in detail with an example. (16)

Or

(b) Explain the various types of hazards in sequential circuit design and the methods to eliminate them. Give suitable examples. (16)

20. (a) Explain in detail the RTL design procedure. (16)

Or

(b) Write a VHDL program and explain the design procedure of 4-bit comparator. (16)

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