Reg. No. : | | | | | | | | | | |

Question Paper Code: 41481

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Elective

Electronics and Communication Engineering

14UEC903 - COMPUTER ARCHITECTURE AND ORGANIZATION

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. The addressing mode which makes use of in-direction pointers is

   (a) Indirect addressing mode (b) Index addressing mode
   (c) Relative addressing mode (d) Offset addressing mode

2. Floating point representation is used to store

   (a) boolean values (b) whole numbers
   (c) real integers (d) integers

3. In computers, subtraction is generally carried out by

   (a) 9’s complement (b) 10’s complement
   (c) 1’s complement (d) 2’s complement

4. Pipeline implement

   (a) fetch instruction (b) decode instruction
   (c) fetch operand (d) calculate operand

5. CPU does not perform the operation

   (a) data transfer (b) logic operation
   (c) arithmetic operation (d) all the above

6. A micro program written as string of 0's and 1's is a

(a) symbolic microinstruction (b) binary microinstruction
(c) symbolic micro program (d) binary micro program

7. The techniques which move the program blocks to or from the physical memory is called as

(a) Paging (b) Virtual memory organization
(c) Overlays (d) Framing

8. The associatively mapped virtual memory makes use of

(a) Translation Look-aside Buffer (b) Page table
(c) Frame table (d) None of these

9. Interrupts which are initiated by an instruction are

(a) internal (b) external (c) hardware (d) software

10. The computer architecture aimed at reducing the time of execution of instructions is

(a) CISC (b) RISC (c) ISA (d) ANNA

PART - B (5 x 2 = 10 Marks)

11. Write the general format for floating point numbers.

12. What is coprocessor and what are the functions performed by the coprocessor?

13. What is an instruction pipeline?

14. Differentiate between static and dynamic RAM.

15. Define handshaking related to the data transfer.

PART - C (5 x 16 = 80 Marks)

16. (a) What are the different types of CPU organization? Explain with relevant examples. (16)

Or

(b) Explain the different types of addressing modes with suitable examples. (16)

17. (a) With relevant diagram and expressions, explain the operation of carry look ahead adder. (16)

Or

(b) Explain how multiplication is carried out using Booth's algorithm. Extend it for floating point operation. What are the advantages of modified Booth's algorithm? (16)

18. (a) Explain in detail about instruction pipelining with flow chart. (16)

Or

(b) What is associate memory? Draw the block diagram of associate memory and explain how the read and write operations performed in associated memory. (16)

19. (a) Explain preemptive and non-preemptive memory allocation strategies in detail. (16)

Or

(b) Write short notes on multilevel memories and optical memories. (16)

20. (a) Draw the typical block diagram of a DMA controller and explain how it is used for direct data transfer between memory and peripherals. (16)

Or

(b) Explain the use of vectored interrupts in processors. Why is priority handling desired in interrupt controllers? How do the different priority schemes work? (16)

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