Reg. No. : | | | | | | | | | | |

Question Paper Code: 31481

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Elective

Electronics and Communication Engineering

01UEC903 - COMPUTER ARCHITECTURE AND ORGANIZATION

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. Discuss the stored program concept.
2. Differentiate direct and indirect addressing mode.
3. Point out the advantages of Co-processors.
4. Discuss the principle behind the Booth's multiplier.
5. What is microprogramming?
6. List the four stages in the instruction pipelining.
7. Write about associative memory.
8. Define memory latency.
9. List out the limitations of the programmed I/O data transfer method.
10. What is memory mapped I/O?

PART - B (5 x 16 = 80 Marks)

11. (a) Briefly explain the organization of CPU and memory of the IAS computer with instruction set. (16)

Or

(b) Explain the operation of each functional unit in the computer system with suitable diagram. (16)

12. (a) State the advantages of sequential ALU over combinational ALU for multiplier and divider operation. Also discuss the structure of basic sequential ALU. (16)

Or

(b) With a neat sketch, explain in detail about logic design for fast adders. (16)

13. (a) Explain the design of micro-programmed control unit for the two's complement multiplier with a diagram. (16)

Or

(b) Explain the super scalar operations with a neat diagram. (16)

14. (a) Explain different types of mapping functions in cache memory. (16)

Or

(b) Explain the concepts of memory hierarchies. (16)

15. (a) List out the three bus arbitration schemes. Explain any two with a diagram. (16)

Or

(b) Explain in detail about standard I/O interfaces. (16)