Reg. No. : | | | | | | | | | | |

Question Paper Code: 31574

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Seventh Semester

Electronics and Instrumentation Engineering

01UEI704 - VLSI SYSTEM DESIGN

(Regulation 2013)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 2 = 20 Marks)

1. What are the second order effects in a MOS transistor?
2. What are the advantages of Twin-tub process?
3. State the significance of Lambda based rule.
4. Indicate the different symbols used for various regions in stick diagram.
5. Distinguish absolute clock skew and relative clock skew.
6. List the few applications of Tally circuits.
7. What factors determine the overall size of a PLA?
8. Mention some of PLDs.
9. List out the operators in VHDL.
10. Write the behavioral VHD L code for a full adder.

PART - B (5 x 16 = 80 Marks)

11. (a) (i) Show the various components of nMOS transistor model. (6)

(ii) Elaborate the process and steps involved in CMOS Fabrication of VLSI system technology. (10)

Or

(b) Explain the operation of MOS transistor in depletion mode and enhancement mode. (16)

12. (a) Explain the DC characteristics and switching characteristics of a CMOS inverter. (16)

Or

(b) Determine the pull-up to pull down ratio for an nMOS inverter driven by another nMOS inverter. (16)

13. (a) (i) What is Barrel shifter and discuss its SHIFT-1 and SHIEFT-2 operation. (8)

(ii) Discuss about dynamic CMOS. (8)

Or

(b) Explain the design and working of carry look ahead adder. (16)

14. (a) (i) Explain the NMOS NAND-NAND PLA realization with a neat stick diagram. (8)

(ii) Discuss about the design of complex PLA. (8)

Or

(b) Explain in detail about planning placement and routing techniques of FPGA. (16)

15. (a) Write a VHDL code to realize the behavioral model and data flow model of a full adder. (16)

Or

(b) Write the VHDL code for Finite State Machine using behavioral and structural modeling. (16)

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