Reg. No. : | | | | | | | | | | |

Question Paper Code: 50233

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Third Semester

Computer Science and Engineering

15UCS303 - COMPUTER ORGANIZATION AND ARCHITECTURE

(Common to Information Technology)

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. Which registers can interact with the secondary storage?

   (a) MAR (b) PC (c) IR (d) R0

2. The instructions like MOV or ADD are called as

   (a) OP – Code (b) Operators (c) Commands (d) None of these

3. The multiplier is stored in

   (a) PC register (b) Shift register (c) Cache (d) None of these

4. The periods of time when the units is idle is called as

   (a) Stalls (b) Bubbles (c) Hazards (d) Both (a) and (b)

5. The logical addresses generated by the CPU are mapped onto physical memory by

   (a) Relocation register (b) TLB (c) MMU (d) None of these

PART - B (5 x 2 = 10 Marks)

6. What is meant by an addressing mode? Mention most important of them.

7. Define the term computer architecture.

8. Sate the rule for floating point addition.

9. Why is branch prediction algorithm needed? Differentiate between the static and dynamic techniques.

10. Write short note on magnetic hard disks.

PART - C (5 x 16 = 80 Marks)

11. (a) Explain different types of instructions with examples. Compare their relative merits and demerits. (16)

Or

(b) Explain the various addressing modes with examples. (16)

12. (a) Explain the non-restoring algorithm for integer division with an example. (16)

Or

(b) Describe the techniques for handling data and instruction hazards in pipelining. (16)

13. (a) Describe the IEEE standards for single and double precision floating point numbers. (16)

Or

(b) Explain a 4-stage instruction pipeline. Also explain the issues affecting pipeline performance. (16)

14. (a) Explain various memory technologies with a suitable example. (16)

Or

(b) Draw the block diagrams of two types of DRAMs and explain. (16)

15. (a) Explain in detail about virtual memory. (16)

Or

(b) Discuss the various mapping techniques used in catch memories. (16)