Reg. No. : | | | | | | | | | | |

Question Paper Code: 50228

B.E. / B.Tech. DEGREE EXAMINATION, MAY 2017

Second Semester

Computer science and Engineering

15UCS208 - DIGITAL PRINCIPLES AND SYSTEM DESIGN

(Common to Information Technology)

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (5 x 1 = 5 Marks)

1. How many bits are required to represent the decimal numbers in the range 0 to 999 using straight binary code

   (a) 8 (b) 10 (c) 12 (d) 16

2. How many full adders are required to construct an m-bit parallel adder?

   (a) m (b) m-1 (c) m+1 (d) m+2

3. The function of a multiplexer is

   (a) To decode information
   (b) to select 1 out of N input data sources and to transmit it to single channel
   (c) to transmit data on N lines
   (d) to perform serial to parallel conversion

4. How many flip flops are required to build a binary counter circuit to count from 0 to 1023?

   (a) 6 (b) 10 (c) 24 (d) 12

5. In PAL, how 10L8 is represented

   (a) 10-I/P L-Active Low Output 8 Outputs
   (b) 10-I/P L-Active Low Input 8 Outputs
   (c) 10-I/P L-Active Low Input Output 8 Outputs
   (d) none of these

PART - B (5 x 3 = 15 Marks)

6. Realize XOR gate using only NAND gates.

7. Obtain the truth table for BCD to Excess-3 code converter.

8. How to design 3-to-8 line decoder using 2-to-4 line decoders?

9. Define state reduction problem with example.

10. Compare asynchronous and synchronous sequential circuit.

PART - C (5 x 16 = 80 Marks)

11. (a) Simplify the following Boolean function by using the Quine–McClusky Method: $F(A,B,C,D) = \sum m(1,2,3,5,9,12,14,15) + \sum d(4,8,11)$. (16)

Or

(b) (i) Add, subtract and multiply the following numbers in binary 101010 and 110010. (6)

(ii) Reduce the following function using K map technique:

$F(A,B,C,D) = \sum m(5,6,7,12,13) + \sum d(4,9,14,15)$ (10)

12. (a) Design a combinational circuit to convert gray code to binary code. (16)

Or

(b) (i) Design a full adder and realize it using only NAND gates. (8)

(ii) Design a 2-bit magnitude comparator. (8)

13. (a) Implement the Boolean function using 8:1 multiplexer

F(A, B, C, D) = AB'D + A'C'D+B'CD'+AC'D. (16)

Or

(b) Design BCD to excess 3 code converter using PAL. (16)

14. (a) Design MOD 8 up/down counter using T- flip flops with necessary diagrams and tables. (16)

Or

(b) (i) Write short notes on shift register with neat diagram. (6)

(ii) Design MOD 6 counter circuit using J-K flip flop. (10)

15. (a) An asynchronous sequential circuit is described by the following excitation and output function

$$X = (YZ'W)X + (Y'ZW')$$

$$S=X'$$

(i) Draw the logic diagram of the circuit

(ii) Derive the transition table and output map

(iii) Describe the behavior of the circuit. (16)

Or

(b) (i) What is the objective of state assignment in asynchronous circuit? Explain race free state assignment with an example. (8)

(ii) Discuss about static, dynamic and essential hazards in asynchronous sequential circuits. (8)

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