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Question Paper Code : 65069

5 Year M.Sc. DEGREE EXAMINATION, MAY/JUNE 2013.

Second Semester

Software Engineering

XIT 121 / 10677 SW 204 – COMPUTER ARCHITECTURE

(Common to 5 Year M.Sc. Information Technology)

(Regulation 2003/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. What are the conditional code flags and what are the commonly used condition code flags?

2. List the technology improvements in the third and forth generation computers.

3. Define Von Neumann rounding.

4. What is bit-pair recording of multipliers?

5. What are the advantages and disadvantages of hardwired control?

6. Define pipeline speedup and pipeline efficiency.

7. How many 128 x 8 RAM chips are needed to provide a memory capacity of 2 MB?

8. Compare RDRAM with DDR SDRAM.

9. List the sequence of events involved in handling interrupt request.

10. What is an I/O interface and why it is required?

PART B — (5 × 16 = 80 marks)

11. (a) (i) Name various registers in the processor and explain their functions. (6)

(ii) Write a program to evaluate the expression A×B + C × D in a signal accumulator processor. Assume that processor has Load, Store, Multiply and Add instructions. (6)

(iii) Compare CISC with RISC architecture in detail. (4)

Or

(b) (i) Discuss about various performance issues in computer systems in detail. (8)

(ii) Consider the various possibilities of saving the return address of a subroutine such as in a processor register, in memory location and on a stack. Which of these possibilities support nesting and which supports recursion? Explain. (8)

12. (a) (i) Design a 4-bit carry look-ahead adder and explain. (8)

(ii) With block diagram, explain the implementation of floating-point operations in detail. (8)

Or

(b) (i) Draw the block diagram of hardware arrangement of multiplication and illustrate with an example how multiplication of number is carried out. (8)

(ii) Show the logic circuit for implementing restoring division and illustrate the restoring division algorithm with suitable example. (8)

13. (a) Discuss about various hazards that cause performance degradation in pipelined processors and the means for mitigating their effects.

Or

(b) (i) Describe the architecture of a typical superscalar processor with the help of block diagram. (8)

(ii) Explain hardwired control unit organization and generation of control signals in detail. (8)

14. (a) (i) Describe by means of a block diagram how multiple matched words can be read out from an associate memory. (8)

(ii) Explain the translation of virtual address into real address with the use of an associate-mapped TLB. (8)

Or

(b) (i) Discuss about the kinds of mapping functions used in cache memory with their advantages and disadvantages. (8)

(ii) Describe the principles of storing and retrieving data in optical disks. (8)

15. (a) (i) Design a parallel priority interrupt hardware for a system with eight interrupt sources. (8)

(ii) Briefly explain the operation of SCSL bus. (8)

Or

(b) (i) Draw the circuit diagram for an input interface and explain. (8)

(ii) Explain how program controlled I/O is performed using polling. (8)