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Question Paper Code : 65106

(5 Year) M.Sc. DEGREE EXAMINATION, MAY/JUNE 2013.

Second Semester

Software Engineering

ESE 022 – COMPUTER ARCHITECTURE

(Regulation 2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What is program control Unit?

2. What is the function of flip-flop?

3. For the 16-bit binary number 1001 0101 1100 0011, show the effect of a right shift of 4 bits with sign extension.

4. What is coprocessor?

5. Define control dependency.

6. What is the difference between Horizontal versus vertical micro instructions?

7. What is cache miss?

8. A computer has 16 pages of virtual address space but only 4 page frames. Initially, the memory is empty. A program references the virtual pages in the order.

   0, 7, 2, 7, 5, 8, 9, 2, 4

   Which reference cause a page fault with LRU.

9. What is busy waiting?

10. Define cycle stealing.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Describe in detail about the evolution of Computers. (8)

(ii) What is the purpose of using stack in the CPU? Explain how it is implemented. (8)

Or

(b) (i) A digital computer has 16 registers, each is of 32 bits. They are connected by a common bus which is constructed with multiplexers.

(1) How many selection inputs are there in each multiplexer? (3)

(2) How many multiplexer are there in the bus? (3)

(3) What sizes of multiplexers are needed? (2)

(ii) What is opcode? Explain th4e instruction code format in detail. (8)

12. (a) (i) Explain about the floating point Arithmetic operation for floating point number. (8)

(ii) Describe the structure of carry-lookahead adder. (8)

Or

(b) (i) Design a multiplier for two's complement fractions. (8)

(ii) Describe the structure of basic sequential ALU. (8)

13. (a) (i) A pipelined processor has two branch delay slots. An optimizing compiler can fill one of these slots 85% of the time and can fill the second slot only 20% of the time. What is the percentage improvement in performance achieved by this optimization, assuming that 20% of the instructions executed are branch instruction? (8)

(ii) Explain the difference between Micro programmed control and Hardwired control. (8)

Or

(b) (i) Assume that a simple CPU has four major phases to its instructions cycle: fetch, indirect, execute and interrupt. Two 1-bit flags designate the current phase in a hardwired implementation.

(1) Why these flags are needed? (4)

(2) Why are they not needed in micro programmed control unit? (4)

(ii) Explain the steps involved to execute complete instructions with a diagram. (8)

14. (a) (i) A two-level memory system has eight virtual pages on a disk to be mapped into four page frames in the main memory. Assume the page frames are initially empty. During execution, a certain program generated the following page trace :

1, 2, 0, 2, 1, 7, 7, 6, 0, 1, 2, 0, 3, 0, 4, 5, 1, 5, 2, 4, 5, 6, 7, 6, 2, 4, 7, 3, 2, 4, 4

Show the successive virtual pages residing in the four page frames with respect to the above page trace using the circular FIFO page replacement policy. Compare the hit ratio in the main memory. (8)

(ii) Describe with neat diagram for Not-Recently-used page replacement policy. (8)

Or

(b) (i) The memory unit of a computer system is 128K × 16 and is having a cache memory of 2K words. The cache memory uses direct mapping with a block size of four words.

(1) How many bits are there in the tag, index, block and word fields of the address format? (4)

(2) How many bits are there in each word of cache, and how are they divided into functions? Include a valid bit in the format. (4)

(ii) Explain about Least Recently used page replacement policy with a diagram.

15. (a) (i) What is system bus? How CPU, Memory and I/Os are interconnected? Explain. (8)

(ii) A computer uses DMA to read from the disk. The disk has 64 sectors per track, each sector is of 512 byte. The disk rotation time is 16 msec. The bus is 16 bits wide and bus transfer take 500 nsec each. The average CPU instruction requires two bus cycles. How much is the CPU slowed down by DMA? (8)

Or

(b) (i) Assume a computer without priority interrupt hardware. Any one of the many sources can issue the interrupt that interrupted the computer and any interrupt request results in storing the return address and branching to a common interrupt service routine. Explain how a priority can be established in the interrupt service program? (8)

(ii) What is the different between RISC and CISC processor? (8)

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