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Question Paper Code : 65033

5 Year M.Sc. DEGREE EXAMINATION, MAY/JUNE 2013.

First Semester

Software Engineering

XCS 114/10677 SW 104 — DIGITAL PRINCIPLES

(Common to 5 Year M.Sc. Information Technology and
5 Year M.Sc. Computer Technology)

(Regulation 2003/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert the decimal numbers 68 and 0.4375 to binary numbers.

2. Simplify the following Boolean expression to minimum number of literals.

   Y = ABC + A'B+ ABC'

3. Simplify the following Boolean functions using three variable maps.

   $F(A, B, C) = \Sigma(0,2, 6,7)$.

4. Draw the logic diagram of a 2 to 4 decoder including an enable input using NOR gates.

5. Construct a J-K flip-flop using D-flip-flop.

6. Write HDL behavioural description of D-flip-flop with asynchronous reset.

7. What are the general capabilities of the shift register?

8. What are the difference between ring counter and Johnson counter?

9. Draw the logic circuit and truth table of S-R latch using NAND gates.

10. What is Hazard in combinational circuit? Explain with an example

PART B — (5 × 16 = 80 marks)

11. (a) (i) Perform the following binary division in binary. (4)

1011111 ÷ 101

(ii) Add and multiply the hexadecimal numbers 2E and 34 without converting to decimal. (6)

(iii) Represent the decimal numbers 6027 and 4256 in BCD, excess-3 code and 2421 code. (6)

Or

(b) (i) The Boolean function $F = xy'z + x'y'z + w'xy + wx'y + wxy$. (8)

Simplify the function to a minimum number of literals and obtain the truth table.

Draw the logic diagram for the simplified expression.

(ii) Convert the following expression into sum of products and products of sum. (8)

$Y = x' + x(x + y')(y + z')$.

12. (a) (i) Simplify the following Boolean function using five variable map. (10)

F (A, B, C, D, E) = (0, 2, 4, 6, 9, 13, 21, 23, 25, 29, 31)

(ii) Write the HDL description of the circuit for the following Boolean function. (6)

$x = A(CD + B) + BC'$

Or

(b) (i) Design a binary multiplier that multiplies two 4-bit numbers. Use AND gates and binary adders. (10)

(ii) Implement the following Boolean function with a multiplexer. (6)

$F(x, y, z) = \Sigma(1, 2, 6, 7)$

13. (a) A sequential circuit with two D-flip-flops A and B, two inputs x and y and one output z is specified by the following next-state and output equations

$A(t+1) = x'y + xA$

$B(t+1) = x'B + xA$

$z = B$

(i) List the state table for the sequential circuit. (6)

(ii) Draw the corresponding state diagram. (6)

(iii) Draw the logic diagram of the circuit. (4)

Or

(b) A sequential circuit has three flip-flops A, B, C, one input x and one output y. The state diagram is given in Figure-1. The circuit is to be designed by treating the unused states as don't care conditions using J-K flip-flops. (16)

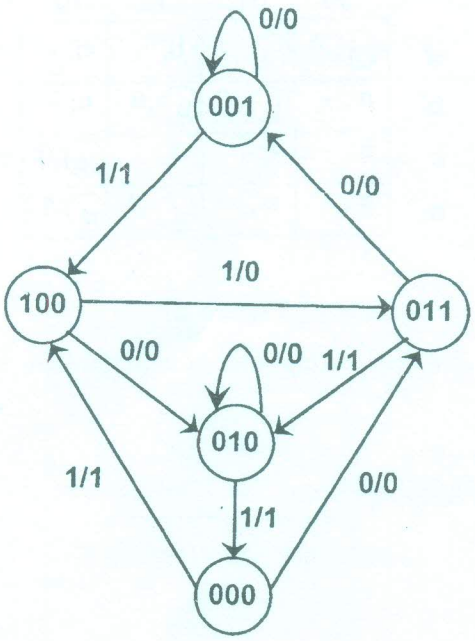

Figure 1

14. (a) (i) Design a serial adder using shift register. (8)

(ii) Design a three bit BCD ripple counter using J-K flip-flops. (8)

Or

(b) (i) Design a counter with the following repeated binary sequences using D-flip-flops. (8)

$y = (0, 1, 2, 4, 6)$

(ii) Write HDL behavioural and structural description of ripple counter. (8)

15. (a) An asynchronous sequential circuit has two internal states and one output. The excitation and output function describing the circuit are.

$Y_1 = x_1 x_2 + x_1 y_2' + x_2' y_1$

$Y_2 = x_2 + x_1 y_1' y_2 + x_1' y_1$

$z = x_2 + y_1$

(i) Derive the transition table and output map. (6)

(ii) Obtain the flow table for the circuit. (6)

(iii) Draw the logic diagram of the circuit. (4)

Or

(b) (i) Obtain a binary state assignment for the reduced flow table shown in Figure 2. Avoid critical race conditions. (8)

	x_1x_2 = 00	01	11	10
a	(a),0	(a),1	b, -	d, -
b	a, -	(b),0	(b),0	c, -
c	a, -	-, -	d,-	(c),0
d	a, -	a, -	(d),1	(d),1

Figure 2

(ii) Obtain the logic diagram of the circuit using NAND latches and gates. (8)