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Question Paper Code : 65102

5 Year M.Sc. DEGREE EXAMINATION, MAY/JUNE 2013.

First Semester

Computer Technology

ECT 011/ ESE 012/ EIT 021 – DIGITAL PRINCIPLES

(Common to : 5 Year M.Sc. Information Technology/ 5 Year M.Sc. Software Engineering)

(Regulation 2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Convert Gray code 11011 to equivalent binary code.

2. Simplify y=((AB)' + A' +AB)'.

3. Convert to POS given SOP of F= a'b'c +a'b'c+a'bc+ab'c+abc.

4. Draw the logic diagram for a 2- bit magnitude comparator.

5. Why is state reduction needed?

6. Differentiate between Moore and Mealy Machine.

7. Compare counter and Register.

8. What is a buffer register?

9. Define cycles and Races.

10. State the Fundamental mode of operation.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Draw equivalent of all basic gates using only NAND Gates. (5)

(ii) State and explain Demorgan's Theorem. (6)

(iii) State the Principle of Duality. (5)

Or

(b) What is the need for codes? List its Advantages and Applications? Explain the various codes with suitable examples. (16)

12. (a) (i) Write the HDL code for Decimal Adder. (8)

(ii) Obtain the minimal SOP and POS for F = $\sum m(1,3,4,5,6,7,9,12,13)$. (8)

Or

(b) (i) Write the HDL code for an Encoder. (8)

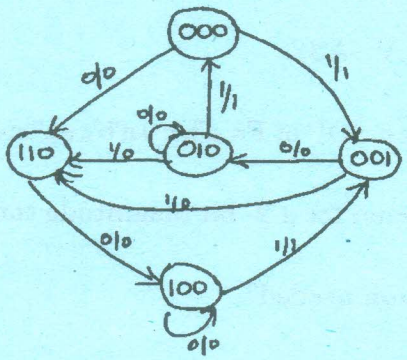
(ii) Minimize the following Boolean expression using k-map and realize it using basic gates F = $\sum m(1,3,5,9,11,13)$. (8)

13. (a) (i) Design a serial Adder. Obtain the logic diagram, derive the truth table and draw the timing diagram.

(ii) Explain the operation of a JK Flip flop.

Or

(b) Implement the following state diagram using D flip – flop.



14. (a) (i) Draw the 4 bit universal shift register using multiplexer and D flip- flop and explain. (8)

(ii) Design a 3 bit binary counter using T flip flop. (8)

Or

(i) Explain Data transfer between register (6)

(ii) Design a binary up-down counter. (10)

15. (a) Design a T flip-flop using logic gates. (16)

Or

(b) Deign an Asynchronous sequential circuit with two inputs X and Y, and one output Z. Whenever Y is 1, input X is transferred to Z. When Y is 0, the output does not change for any change in X. Use SR latch for implementing the circuit. (16)
