LIB
21/6/13 FN

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 71868

M.E. DEGREE EXAMINATION, JUNE/JULY 2013.

First Semester

VLSI Design

VL 9211/VL 911/10244 VLE 13 — DSP INTEGRATED CIRCUITS

(Common to M.E. Applied Electronics, M.E. Digital Signal Processing and M.E. Medical Electronics)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What are the major design steps involved in the direct mapping approach?

2. Sketch the cross section of a silicon gate CMOS inverter in a bulk n-well process.

3. What is the condition for the LSI system to be BIBO stable?

4. List out the applications of Adaptive DSP algorithms.

5. Show that an FIR interpolator can be decomposed into L parallel FIR filters that operate at the input sampling rate and produce a combined output signal with an L times higher sampling rate.

6. Determine Signal-to-noise ratio for the safely scaled 16-point FFT.

7. What is the aim of using complex PEs in DSP?

8. State the basic architectural features of standard DSP processor.

9. What are the applications of cordic algorithm?

10. Show that the negative value of a number x, in one's complement representation can be obtained by inverting all bits in the binary word.

PART B — (5 × 16 = 80 marks)

11. (a) What is the importance of partioning in any circuit design? Discuss different types of partioning in detail. (16)

Or

(b) (i) Define propagation delay in CMOS circuits. Derive the expression for charge time and discharge time. (10)

(ii) Estimate the propagation delay for a CMOS inverter that is loaded with five identical inverters connected in parallel. The wiring corresponds to a load of about 5 fF. Use the following values : (6)

$\mu_n = 4.62 \times 10^{-2}$ m²/Vs, $\mu_p = 1.6 \times 10^{-2}$ m²/Vs , $T_{ox} = 155$ Å

$W_{ndrawn} = 2.0\ \mu$m, $W_{neff} = 0.84\ \mu$m, $L_{ndrawn} = 0.8\ \mu$m, $L_{neff} = 0.8\ \mu$m

$W_{pdrawn} = 20\ \mu$m, $W_{peff} = 1.34\ \mu$m, $L_{pdrawn} = 0.8\ \mu$m, $L_{peff} = 0.96\ \mu$m

$V_{Tn} = 0.84\ V_{Tp} = -0.73$ V and $V_{DD} = 5$ V.

12. (a) (i) How can sampling of analog signals be done? What are the problems faced in sampling and how it can be rectified? Also discuss how to select sampling frequency. (12)

(ii) Define the following : Linear Systems, SI Systems and LSI Systems. (4)

Or

(b) What is DCT? Briefly explain different types of DCT. (16)

13. (a) An analog Cauer filter with Amax = 0.09883 dB (ρ = 15%), Amin = 67.09 dB, fc = 2 kHz and fs = 4.7324 kHz has the following poles and zeros :

$S_{p1} = -1.15102 \cdot 2\pi$ $\quad S_{n1} = \infty$

$S_{p2,3} = -0.2951 \cdot 2\pi \pm j\ 2.1526 \cdot 2\pi$ $\quad S_{n2,3} = \pm j\ 4.9534 \cdot 2\pi$

$S_{p4,5} = -0.86564 \cdot 2\pi \pm j\ 1.4098 \cdot 2\pi$ $\quad S_{n4,5} = \pm j 7.8014 \cdot 2\pi$ [krad/s]

The filter is uniquely described by the notation C051525. Use this filter and the bilinear transformation to design a digital lowpass filter with a passband edge of 32 kHz when the sample frequency is 256 kHz.

(i) What are A_{max}, A_{min}, $\omega_c T$, and $\omega_s T$ for the digital filter? (8)

(ii) Sketch the pole-zero configuration for both the analog and digital filters. (8)

Or

(b) What is the purpose of analyzing Parasitic Oscillation? Describe in detail different types of Parasitic oscillations. (16)

14. (a) (i) Discuss in detail different interconnection topologies in Message-Based Architectures. (8)

(ii) Write short notes on wave front arrays and systolic arrays. (8)

Or

(b) How can the following features can be implemented in shared-memory architectures with Bit-serial PEs?

(i) Minimizing the cost (4)

(ii) Uniform memory access rate (4)

(iii) Balancing the Architectures (4)

(iv) Mode of operation and control. (4)

15. (a) Write Short notes on :

(i) Baugh-Wooley's Multiplier (8)

(ii) Serial/Parallel Multiplier (8)

Or

(b) Discuss different steps involved in design of layout of VLSI circuits. (16)
