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Question Paper Code : 71880

M.E. DEGREE EXAMINATION, JUNE/JULY 2013.

Elective

VLSI Design

VL 9261/AP 954/UAP 9167/10244 VLE 11 — ASIC DESIGN

(Common to M.E. Applied Electronics, M.E. Computer and Communication and M.E. Electronics and Communication Engineering)

(Regulation 2009/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Draw and label the CMOS design rule for poly layer.
2. Distinguish between parasitic and nonideal delays.
3. Draw a Xilinx SRAM configuration cell.
4. What are the advantages and disadvantages of totem pole output as compared with complementary output?
5. Define logic synthesis.
6. Give the advantages of hierarchical design.
7. Compare the applications of functional and timing simulation.
8. Write the importance of test in ASIC design.
9. Mention the applications of design rule check.
10. Write the role of partitioning in ASIC design.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the different types of ASICs and write their applications. (10)

(ii) Draw the ASIC design flow and briefly discuss each steps. (6)

Or

(b) (i) Describe the operation of CMOS flip flop and clocked inverter with neat circuit and timing diagrams. (10)

(ii) Explain the problems caused by the parasitic capacitances of MOS transistors. (6)

12. (a) (i) Explain briefly the antifuse and EPROM technologies with neat diagrams. (8)

(ii) Draw the Xilinx XC4000 family CLB and discuss the Xilinx LCA timing model. (8)

Or

(b) (i) Draw and explain the Xilinx XC4000 family I/O block. (10)

(ii) Give a brief note on the issues related to bringing clock and power onto a chip. (6)

13. (a) (i) Discuss the RC delay in antifuse connections and describe the applications of Elmore's delay model. (8)

(ii) Describe the interconnect schemes used in Altera MAX 5000 and FLEX family with necessary diagrams. How do the above schemes differ from that used in Xilinx EPLD? (8)

Or

(b) (i) Explain the applications of schematic entry with neat diagrams. (10)

(ii) Give a brief note on EDIF syntax. (6)

14. (a) (i) Describe the different types of fault simulation. (10)

(ii) Give a brief note on switch and gate level simulation. (6)

Or

(b) (i) Explain the principle of automatic test pattern generation and describe an algorithm for automatic test vector generation. (10)

(ii) Give a brief note on boundary scan test. (6)

15. (a) (i) Explain the application of Kernighan-Lin algorithm in partitioning. (10)

(ii) Compare the principle of constructive and iterative placement improvement algorithms. (6)

Or

(b) (i) Explain the special routing in an ASIC. (8)

(ii) Compare the goals and objectives of global and detailed routing. Give a brief note on the principle of multilevel and timing-driven routing methods. (8)
