LIB
27/5/13 FN

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 21480

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2013.

Fourth Semester

Instrumentation and Control Engineering

IC 2251/IC 43/EC 1263 A/10133 IC 403/080260004 — DIGITAL PRINCIPLES AND DESIGN

(Regulation 2008/2010)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Design a half adder using logic gates.

2. Realize the function $F = \Sigma m(0, 1, 3, 6, 7)$ using 8 : 1 multiplexer.

3. How will you convert JK flipflop into D and T flipflops?

4. Design a 3-bit ring counter.

5. Realise the given functions using suitable decoder

   $F_1 = \Sigma m(1, 2, 4, 6)$

   $F_2 = \Sigma m(0, 2, 3, 4, 5)$.

6. Draw the architecture of a general FPGA.

7. Draw a two input NAND gate using TTL and CMOS logic families.

8. Define propagation delay.

9. Why is CMOS preferred over NMOS technology?

10. Write the applications of ECL and I^2L logic families.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Simplify the given Boolean function using Quine Mccluskey method and draw the logic diagram using gates for the simplified Boolean expression.

$F = \Sigma m(0, 3, 4, 5, 6, 7, 9, 10, 14)$. (12)

(ii) Realise XOR function using NAND-NAND logic. (4)

Or

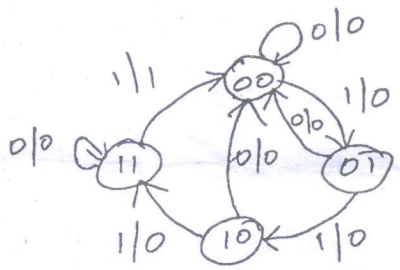
(b) (i) Design a 4 bit binary adder/subtractor and explain its operation. (8)

(ii) Design a 4 bit binary to gray code converter. (8)

12. (a) Design a 4 bit up/down synchronous counter using JK flipflops and explain its operation. (16)

Or

(b) For the given state diagram design a sequential circuit using D flipflops.



13. (a) Realise the given functions using suitable PAL device

$F_1 = \Sigma m(0, 1, 2, 5, 6, 9, 11)$

$F_2 = \Sigma m(1, 3, 5, 7, 10, 13, 15)$. (16)

Or

(b) Design a sequence detector which detects the sequence 11011 using PAL device. (16)

14. (a) What is the function of a pull up resistor when interfacing TTL IC to CMOS IC? Describe with an example. (16)

Or

(b) Why ECL is called non-saturating logic? With the help of circuit diagram describe the operation of ECL OR/NOR logic. (16)

15. (a) With a neat diagram explain the operation of a CMOS inverter. (16)

Or

(b) Describe the operation of a nMOS inverter with neat diagrams. (16)
