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6.6.13 AN

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Question Paper Code : 21296

B.E/B.Tech. DEGREE EXAMINATION, MAY/JUNE 2013.

Seventh Semester

Electrical and Electronics Engineering

CS 2071 / CS 608 – COMPUTER ARCHITECTURE

(Common to Electronics and Instrumentation Engineering and
Instrumentation and Control Engineering)

(Regulation 2008)

Time : Three hours

Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. What do you mean by direct addressing?
2. Write the types of instruction sets.
3. What is the multiply rule for floating point numbers?
4. Draw the diagram of a basic cell that can be used in each bit stage of an adder.
5. Write the steps involved in executing the instruction Move (R1), R2.
6. Draw the diagram for a 4 – stage Pipeline.
7. What is the significance of Cache memory?
8. Define Paging.
9. What do you mean by Bus arbitration technique?
10. Define Interrupt.

PART B — (5 × 16 = 80 marks)

11. (a) (i) Explain the basic concepts in Instruction formats and comment on the tradeoffs in it. (8)
- (ii) Write a program using IA32 instruction set to read a line of character and display it. (8)

Or

- (b) Describe the different types of addressing modes and give example for each. (16)
12. (a) (i) Explain the concept of Addition and Subtraction of Signed Numbers with suitable examples. (8)
- (ii) Design and explain 4 – bit Carry look ahead Adder. (8)

Or

- (b) (i) Explain the IEEE standard for Floating point number with diagram. (6)
- (ii) Explain the Booth algorithm for multiplying two numbers with simple example. (10)
13. (a) (i) Explain the Control sequence for execution of the instruction Add (R3), R1. (8)
- (ii) Write detailed notes on Micro programmed control. (8)

Or

- (b) (i) Explain the different addressing modes in pipelining. (8)
- (ii) How does the use of pipeline stages improve the computer's performance? What are pipeline hazards and how are they prevented from happening? (8)
14. (a) Describe the different types of memories. (16)

Or

- (b) (i) Explain the Data storage and retrieval principles of Optical Disks. (8)
- (ii) Illustrate the address translation mechanism used in virtual memories. (8)

15. (a) (i) Explain the Accessing mechanism of I/O Devices.
(ii) Explain the Enabling and Disabling Interrupts mechanism handled by a processor. (8)

Or

- (b) Define DMA. Explain the process of DMA with necessary buses and interfaces. (16)
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