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**Question Paper Code : 21398**

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2013.

Fourth Semester

Electrical and Electronics Engineering

EE 2254/EE 45 /EC 1260/10133 EE 405/080280028 – LINEAR INTEGRATED CIRCUITS AND APPLICATIONS

(Common to Instrumentation and Control Engineering and Electronics and Instrumentation Engineering)

(Regulation 2008/2010)

(Also common to PTEE 2254 – Linear integrated circuits and applications for B.E(Part– Time ) Third Semester – Electronics and Instrumentation Engineering – Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. List the advantages of integrated circuit over discrete component circuit.

2. Explain why inductors are difficult to fabricate in IC'S.

3. What are the different linear IC Packages?

4. What is the input impedance of a non-inverting amplifier?

5. List the applications of analog multipliers.

6. Write the significance of lock range of a PLL.

7. Define the terms settling time and conversion time related to DAC's.

8. What is the function of a voltage regulator?

9. What is the principle of switch mode power supplies?

10. How many resistors are required in a 12-bit weighted resistor DAC?

PART B — ($5 \times 16 = 80$ marks)

11. (a) Describe the Epitaxial growth process and photolithography process with neat diagram.

Or

(b) Give the various ways for making integrated resistor.

12. (a) List the six characteristics of an ideal op-amp and explain in detail. Give the practical op-amp equivalent circuit.

Or

(b) Explain in detail about DC characteristics of op-amp.

13. (a) Explain the principle of Instrumentation amplifier and derive the gain for that circuit.

Or

(b) With neat sketches explain in detail about I/V and V/I converter using op-amp.

14. (a) Design a first order low pass filter for a high cut-off freq of 2 KHz and pass band gain of 2.

Or

(b) Explain the operation of a square wave generator by drawing the capacitor and output voltage wave forms.

15. (a) Design an adjustable voltage regulator (5V to 15 V) with a short circuit current limit of 50MA using a 723 regulator.

Or

(b) Design a 4 bit R– 2R ladder network, determine the size of each step if $r = 10k\Omega$, $R_f = 40\,k\Omega$ and Vcc = ± 15V. Calculate the output voltage for $D_o = 1$, $D_2 = 1$, $D_3 = 1$ if bit '1' applied as 5V and bit '0' applied as OV.