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Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 21433

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2013.

Eighth Semester

Electrical and Electronics Engineering

EI 2403/EI 73 – VLSI DESIGN

(Common to Seventh Semester – Electronics and Instrumentation Engineering and Eighth Semester – Instrumentation and Control Engineering)

(Regulation 2008/2010)

Time : Three hours | Maximum : 100 marks

Answer ALL questions.

PART A — ($10 \times 2 = 20$ marks)

1. Write the equation for drain current of NMOS transistor considering the channel length modulation effect.

2. What are the factors that cause drain punch through in MOS transistors?

3. What are the drawbacks of NMOS inverters compared with CMOS inverters?

4. Write the pull up/pull down ratio required when an inverter is driven through pass transistors.

5. Mention the function and applications of tally circuits.

6. What are the advantages of dynamic CMOS logic structures?

7. Write the two special classes of FPLA.

8. What are the factors that determine the overall size of a PLA?

9. Write the VHDL entity and architecture for a two input AND gate.

10. What does a package consist of? Write the primary purpose of a package.

PART B — ($5 \times 16 = 80$ marks)

11. (a) (i) Explain the different steps involved in NMOS fabrication process with neat diagrams. (8)

(ii) An NMOS transistor has the following parameters: gate oxide thickness = 10 nm, relative permittivity of gate oxide = 3.9, electron mobility = 520 cm^2/V-sec and threshold voltage = 0.7 V. The permittivity of free space = 8.85 x 10^{-14} F/cm. Calculate the gate capacitance and also determine the drain current when V_{GS} = 2V and V_{DS} = 3V. The width (W) and length (L) of the channel are 10 μm and 0.5μm respectively. (3+5)

Or

(b) (i) Explain the small signal model of MOS transistors with neat diagram and expressions. (8)

(ii) Explain the significance of threshold voltage and body effect with their equations. (8)

12. (a) (i) Draw the stick diagram and layout of a NMOS inverter. (8)

(ii) Explain the operation of an inverting and a noninverting NMOS superbuffer. (8)

Or

(b) (i) Draw and explain the operation of a BiCMOS inverter and a two input BiCMOS NOR gate. (4+6)

(ii) Give a brief note on the theory and design of pass transistor logic.(6)

13. (a) (i) Describe the operation of an NMOS and a CMOS exclusive-OR structure. (8)

(ii) Explain the various methods to improve the speed of four bit adders. (8)

Or

(b) (i) Explain the operation of 4×4 NMOS barrel shifter with neat diagrams. (8)

(ii) Draw and explain the NMOS and CMOS implementation of a 4 to 1 MUX. (8)

14. (a) (i) Explain the NMOS NAND-NAND PLA realization and illustrate its application with suitable examples and neat diagrams. (10)

(ii) Write a brief note on dynamic logic arrays. (6)

Or

(b) (i) Describe the implementation of clocked FSM using PLA and write its applications. (8)

(ii) Explain the programmable interconnects and I/O blocks used in FPGA. (8)

15. (a) (i) Write the VHDL description of a 4 bit ripple counter. (8)

(ii) Explain the data types and operators supported by VHDL. (8)

Or

(b) (i) Explain the different sequential statements available in VHDL. (10)

(ii) Discuss the declaration of VHDL function and procedure with suitable examples. (6)