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**Question Paper Code : 21373**

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2013.

Sixth Semester

Electronics and Communication Engineering

EC 2354/EC 64 – VLSI DESIGN

(Regulation 2008)

(Common to PTEC 2354 – VLSI Design for B.E. (Part-Time) Fifth Semester – Electronics and Communication Engineering – Regulation 2009)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. List the various issues in Technology-CAD.

2. Define the lambda layout rules.

3. What is meant by design margin?

4. How do you define the term "device modeling"?

5. List the various power losses in CMOS circuits.

6. Enumerate the features of synchronizers.

7. List the basic types of CMOS testing.

8. What is meant by logic verification?

9. Give the comparison between structural and switch level modeling.

10. What are gate primitives?

PART B — (5 × 16 = 80 marks)

11. (a) Explain in detail about the ideal I-V characteristics and non ideal I-V characteristics of a NMOS and PMOS devices. (16)

Or

(b) (i) Explain in detail about the body effect and its effect in NMOS and PMOS devices. (8)

(ii) Derive the expression for DC transfer characteristics of CMOS inverter. (8)

12. (a) (i) Explain in detail about the scaling concept and reliability concept. (8)

(ii) Describe in detail about the transistor sizing for the performance in combinational networks. (8)

Or

(b) Discuss in detail about the resistive and capacitive delay estimation of a CMOS inverter circuit. (16)

13. (a) Explain in detail about the pipeline concepts used in sequential circuits. (16)

Or

(b) Discuss the design techniques to reduce switching activity in a static and dynamic CMOS circuits. (16)

14. (a) Explain the design for testability (DFT) concepts. (16)

Or

(b) Explain the following terms,

(i) Silicon debug principles (8)

(ii) Boundary scan technique. (8)

15. (a) Design and develop the HDL project to realize the function of a priority encoder using structural model. (16)

Or

(b) (i) Write a data-flow model verilog HDL program for the two input comparator circuit. (8)

(ii) Write a behavioral level verilog HDL program for the 1×8 multiplexer circuit. (8)

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