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1.6.13 AN

Reg. No. : | | | | | | | | | | | | |

Question Paper Code : 23400

B.E./B.Tech. DEGREE EXAMINATION, MAY/JUNE 2013.

Seventh Semester

Electronics and Communication Engineering

EC 1401 — VLSI DESIGN

(Regulation 2004/2007)

(Common to B.E. (Part-Time) Sixth Semester Regulation 2005)

Time : Three hours Maximum : 100 marks

Answer ALL questions.

PART A — (10 × 2 = 20 marks)

1. Define SSI, MSI, LSI and VLSI.

2. What are the different tools available in a typical CAD tool set?

3. Define threshold voltage of a CMOS transistors.

4. Define noise margin of a CMOS inverter.

5. Define Mealy network.

6. Write the HDL coding for Modulo 2 Adder.

7. What is bubble pushing?

8. What is data path library?

9. List the techniques of Ad-Hoc testing.

10. What is IDDQ testing?

PART B — (5 × 16 = 80 marks)

11. (a) Explain in detail the silicon on insulator process with a neat sketch.

Or

(b) Design the layout for NAND gate and discuss about layout design rules.

12. (a) What is meant by channel length modulation? Explain.

Or

(b) Derive the equation for threshold voltage in PMOS enhancement transistor.

13. (a) Explain the different types of timing control present in verilog with suitable examples. (16)

Or

(b) Write a verilog code for 4 bit priority encoder, 8 : 1 multiplexer and ripple carry adder. (16)

14. (a) (i) Explain programmable interconnect. (8)

(ii) Realise the digital equation using CMOS transistors $y = pq + \overline{rs}$. (8)

Or

(b) Write notes on :

(i) Full custom ASIC (8)

(ii) XilinX programmable Gate Array. (8)

15. (a) Explain the scan-based test techniques. (16)

Or

(b) Explain the following terms :

(i) Fault models (8)

(ii) ATPG (4)

(iii) Statistical Fault Analysis. (4)