A **Reg. No. :**

Question Paper Code: 53306

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Third Semester

Electrical and Electronics Engineering

15UEE306 -DIGITAL LOGIC CIRCUITS

(Regulation 2015)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. Convert gray code 10001011 into binary. CO1-U

   (a) $(11110000)_2$ (b) $(01110101)_2$ (c) $(11100010)_2$ (d) $(11110010)_2$

2. The expansion of ECL is CO1- R

   (a) Emitter-collector logic (b) Emitter-complementary logic

   (c) Emitter-coupled logic (d) Emitter Common logic

3. The process of eliminating the redundant states from the state diagram is known as CO2- U

   (a) State transition (b) State assignment (c)State reduction (d) State realization

4. Full adder has CO2- R

   (a) 1 inputs (b) 2 inputs (c) 3 inputs (d) 4 inputs

5. When both inputs are high, then output of JK flip-flop will be CO3-U

   (a) 0 (b) 1 (c) No change (d) Toggle

6. A flip- flop can store _________ bit data CO3-U

   (a) one (b) two (c) three (d) four

7. Output state in asynchronous sequential logic circuit changes when CO4-U

   (a) Input changes (b) Clock pulse is high

   (c) Input and clock pulse change (d) Clock pulse is low

8. The fastest saturated logic family is ___________. CO4- R

(a) TTL (b) ECL (c) MOS (d) CMOS

9. VHDL stand for CO5- R

(a) Verilog hardware description language

(b) VHSIC hardware description language

(c) Very hardware description language

(d) VMEbus description language

10. Which of the following keyword defines a one dimensional array with elements of the bit datatype? CO5- R

(a) bit (b) boolean (c) bit _vector (d) integer

PART – B (5 x 2= 10 Marks)

11. List the important characteristics of digital logic families. CO1- U

12. Define Decoder CO2- U

13. Distinguish between flip flop and latch. CO3- R

14. Why is state reduction necessary? CO4- R

15. List out the level of abstractions in VHDL. CO5- R

PART – C (5 x 16= 80 Marks)

16. (a) (i) Perform 597-239 in XS-3 code using the 10's complement method. CO1-C (12)

(ii) The message below coded in the 7-bit Hamming code is transmitted through a noisy channel. Decode the message assuming that at most a single error occurred in each code word. CO1-App (4)

1001001, 0111001, 1110110, 0011011

Or

(b) (i) Convert 1100101_2 to its equivalent decimal, octal and hexadecimal value. CO1-App (4)

(ii) State the important characteristics of ECL gates. Draw and explain the 2 input ECL OR/NOR gate.. CO1-U (12)

17. (a) Simplify the following Boolean function by using a Quine-Mccluskey method. $F(A,B,C,D) = \sum m(0,2,3,6,7,8,10,12,13)$. CO2-App (16)

Or

	(b)	(i) Design and realize full adder using basic logic gates.	CO2-App	(8)
		(ii) Design and realize 4:1 multiplexer using basic logic gates.	CO2-App	(8)
18.	(a)	Design and Implement a Mod-5 Synchronous counter using JK flip flops.	CO3-Ana	(16)
		Or		
	(b)	Explain how the JK flip is converted into D and T flip flop.	CO3-C	(16)
19.	(a)	The output (y) of an asynchronous sequential circuit must remain 0 as long as one of its two inputs x_1 is 0. While $x_1 = 1$, The occurrence of first change in another input x_2, should give $y = 1$ as long as $x_1 = 1$ and becomes 0 where x_1 returns to 0. Construct a primitive flow table and reduce the state.	CO4-C	(16)
		Or		
	(b)	Realize the following Boolean functions using PLA and PAL. $Y_1 = \Sigma_m (1,2,4,5,6)$, $Y_2 = \Sigma_m (0,1,6,7)$, $Y_3 = \Sigma_m (2,6)$	CO4-C	(16)
20.	(a)	Write a VHDL program in behavioural description of 4 bit up down counter using if else statement with logic diagram and truth table.	CO5-U	(16)
		Or		
	(b)	(i) Write a HDL code for realizing JK FF in behavioral modeling.	CO5-C	(8)
		(ii) Write a HDL code for realizing half adder in behavioral modeling.	CO5-C	(8)