Reg. No. : | | | | | | | | | | |

Question Paper Code: 43306

B.E. / B.Tech. DEGREE EXAMINATION, APRIL 2019

Third Semester

Electrical and Electronics Engineering

14UEE306 – DIGITAL LOGIC CIRCUITS

(Regulation 2014)

Duration: Three hours Maximum: 100 Marks

Answer ALL Questions

PART A - (10 x 1 = 10 Marks)

1. Convert $(10111.10)_2$ to decimal equivalent

   (a) $(23.5)_{10}$ (b) $(46.5)_{10}$ (c) $(23.2)_{10}$ (d) $(46.2)_{10}$

2. How many binary numbers are created with 8 bits?

   (a) 128 (b) 256 (c) 64 (d) 32

3. How many select lines are contained in multiplexer with 1024 inputs and one output

   (a) 20 (b) 10 (c) 15 (d) 28

4. AND-OR realization is equivalent to

   (a) SOP (b) POS (c) K-map (d) None of these

5. Race around condition occurs in JK flip-flop if

   (a) J=1,K=1 (b) J=0,K=0 (c) J=0,K=1 (d) J=1,K=0

6. In the toggle mode a JK flip-flop has

   (a) J = 0, K = 0 (b) J = 1, K = 1 (c) J = 0, K = 1 (d) J = 1, K = 0

7. Which of the following is a type of shift register counter?

(a) Decade (b) Binary (c) Ring (d) BCD

8. Which of the statement is true about static-1 hazard?

(a) output goes momentarily goes to 0 when it should remain at 1
(b) output goes momentarily goes to 1 when it should remain at 0
(c) output changes 3 or more times
(d) none of these

9. The example of sequential circuit is

(a) Counter (b) 7-segment display
(c) Combinational logic circuit (d) Shift register

10. Main component of a VHDL description are

(a) Entry and Package (b) Entry and Architecture
(c) Package and Architecture (d) Package and Configuration

PART - B (5 x 2 = 10 Marks)

11. Define fan-in and fan-out.

12. Why is MUX called as data selector?

13. List the applications of the flip-flop.

14. What is a hazard?

15. List the data objects supported by VHDL.

PART - C (5 x 16 = 80 Marks)

16. (a) (i) Explain Gray code and Binary code. (8)

(ii) Design a TTL logic circuits for a 2 input NANAD gate. (8)

Or

(b) (i) Convert 1010111011101100_2 into octal, decimal and hexadecimal equivalent. (8)

(ii) List the advantages of digital ICs. (8)

17. (a) Design a full adder using two half-adders and an OR gate. (16)

Or

(b) Minimize the following Boolean function using K map

$F = \Sigma m\,(0, 2, 5, 7, 8, 10, 13, 15, 16, 21, 23, 24, 26, 29) + \Sigma d(1, 9, 18, 30, 31)$

(16)

18. (a) Design a synchronous counter to count the sequence 0 - 1 - 2 - 4 5 - 6 - 0 using JK flip flop. (16)

Or

(b) (i) Design a serial adder using Mealy state model. (8)

(ii) List and explain the steps used for analyzing a synchronous sequential circuit. (8)

19. (a) Explain the various types of hazards in sequential circuit design and methods to eliminate them. Give suitable examples. (16)

Or

(b) (i) An asynchronous sequential circuit is described by the following excitation and output function.

$Y=x_1\ x_2'+(x_1 + x_2')y$

$Z=y$

(1) Draw the logical diagram of the circuit

(2) Derive the transition table and output map.

(3) Obtain flow table. (8)

(ii) Implement the following function using PLA $F_1 = \sum m\,(4,5,7)$ and

$F_2 = \sum m\,(3,5,7)$. (8)

20. (a) Explain the structural VHDL description for a 2 to 4 decoder in details. (16)

Or

(b) Write a VHDL description of a D flip flop. (16)